A Comparative Analysis of Three-Phase Phase-Locked Loops for Grid-Connected Systems

Filip Bakić, Lazar Stojanović, Katarina Obradović, Emilija Lukić

***Abstract*—In renewable power generation system, synchronization of the inverter and the power grid is essential for the stable control of grid-connected inverters. Phase-Locked Loops (PLL) are widely used for grid synchronization due to simple implementation and robust performance against the grid disturbances. The main goal of this paper is to present a survey of the comparative performance evaluation among the synchronous reference frame PLL (SRF-PLL), Lag-PLL, stationary-frame based enhanced PLL (SF-EPLL) and double second-order generalized integrator PLL (DSOGI-PLL) under disturbances such as frequency changes, voltage sags and harmonic distortion. System structures and working principles are presented. Moreover, the parameters design for each algorithm are proposed. Dynamic analysis and experimental results of steady state performance of PLLs are observed and compared to verify and validate theoretical comparative analysis.**

***Index Terms*—Phase-locked loop, grid synchronization, frequency estimation, three-phase**

I. Introduction

Over the past couple of decades, there is a clear trend of switching from fossil fuels to renewable energy sources (RES) in electricity production. Furthermore, distributed generation (DG) of RES and their wide prevalence created a possibility to work independently from the grid i.e. in islanded mode, but also as generating units that inject active or reactive power directly to the grid. Many such grid-tied solutions rely on the proper usage of DC-AC power converters in order to successfully connect to the power system. Hence, advancing both hardware and control solutions has become a great deal.

The process of connecting the inverter to the grid is called synchronization of the inverter. In order to achieve successful synchronization, it is important that amplitude, phase and the frequency of the inverter's and the grid's voltages are precisely determined. In case of small DG such as rooftop solar PV systems intended to connect to weak distribution grid, parameters and quality of grid's voltage can vary significantly due to constant change of load. Thus, robust, efficient and precise controlling scheme becomes even more important.

The research work for the most suitable way for synchronizing inverters with the grid has resulted in numerous solutions. In general, all these methods could be classified as either single phase or three-phase based methods. Some of them, such as open transition transfer, are less applicable due to reduced reliability of the power system. On the other side, others, such as passive synchronization, imply usage of synchoncheck relay for synchronization check of voltage, frequency and phase [1]. Although passive synchronization methods do not require control mechanism, using this type of synchronization results in longer reconnecting process. Nevertheless, the most commonly used synchronization method is active synchronization. With implementation of controlling mechanisms, synchronization can be done by controlling the frequency and voltage. The most acknowledged concepts nowadays are Frequency Locked Loop [2], Droop Control [3], [4] and Phase Locked Loop (PLL). Due to simplicity, robustness and effectiveness in various grid conditions, PLL is the most commonly used synchronization method. To improve PLL performances under various grid conditions, numerous modifications have been done, such as Synchronous Reference Frame PLL (SRF-PLL) [5], enhanced PLL (EPLL), fixed-reference frame PLL (FRF-PLL) [6], Lag-PLL, SF-EPLL and DSOGI-PLL [7] .

In this paper, multiple PLL solutions are introduced and discussed. In the third paragraph PLL algorithms Synchronous Reference Frame PLL (SRF-PLL), Lag-PLL, SF-EPLL and DSOGI-PLL are analyzed. Then, Paragraph IV The process of selection of the adequate parameters for each algorithm is explained. Finally, experimental results were conducted on real prototype of grid-connected inverter.

II. Generalized structure of PLL

Basic structure of every PLL can be organized in three sections, Fig. 1:

1) Phase detector (PD): It compares generated signal with desired one and generates corresponding error. For three-phase systems, voltages u_{abc} in a stationary reference frame are transformed in a synchronous rotating frame, where sinusoidal voltages are represented as DC values u_{dq}.
2) Low-Pass filter (LPF): Some phase detectors generate undesired high frequency signals that need to be filtered. For three-phase systems, LPF is often designed as PI controller which input is q component of the voltage. The goal for PI controller is to bring q component to zero. This will ensure that phase is aligned with d axis.
3) Voltage controlled oscillator (VCO): After the angular frequency is estimated, it is integrated to get phase. This phase is then sent to phase detector to finish one iteration of PLL.

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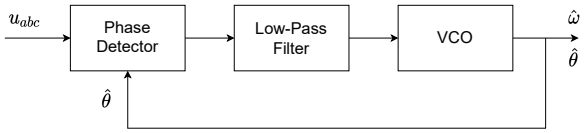

Fig. 1. Basic structure of PLL

III. Overview of the Three-Phase PLL Algorithms

A. SRF-PLL

Synchronous Reference Frame PLL is one of most commonly used algorithm due to its low complexity and easy digital realization. Conventional scheme of the SRF-PLL is shown on Fig.2. Phase detector is cascade Clark (1) and Park (2) transformation. Angle used in Park transformation θ is one estimated from algorithm in previous cycle.

$$T_{abc/\alpha\beta} = \begin{bmatrix}\alpha\\ \beta\end{bmatrix} = \frac{2}{3}\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\begin{bmatrix}a\\ b\\ c\end{bmatrix} \tag{1}$$

$$T_{\alpha\beta/dq} = \begin{bmatrix}d\\ q\end{bmatrix} = \begin{bmatrix}\cos(\theta) & \sin(\theta)\\ -\sin(\theta) & \cos(\theta)\end{bmatrix}\begin{bmatrix}\alpha\\ \beta\end{bmatrix} \tag{2}$$

The goal of this PLL is to bring q component to zero and align the voltage vector with d axis. It is achieved by utilizing PI controller which output is angular frequency. A stationary value of frequency is added to ensure faster phase tracking. Frequency is then integrated to obtain phase, which is then used in PD.

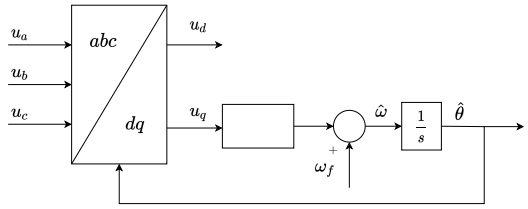

Fig. 2. Scheme of SRF-PLL

B. Lag-PLL

Another implementation of the PLL is shown in Fig.3 as proposed in [8] and referred as Lag-PLL, is derived from SRF-PLL by passing u_q through low-pass filter prior to the PI regulator. The intention of signal filtering is to improve PLL performance when sensing noise and higher harmonics are present in grid voltages.

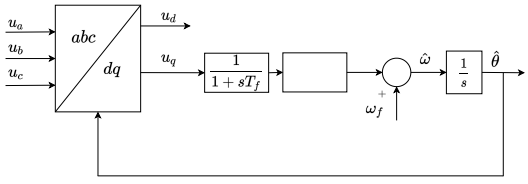

Fig. 3. Scheme of Lag-PLL

C. SF-EPLL

Since standard EPLL algorithm is implemented in a three-phase stationary it is relatively complex due to trigonometric and multiplying operations, the presented algorithm reduces complexity by transforming voltages in $\alpha\beta$ frame. Fig.4 shows the three-phase implementation of the enhanced PLL which was proposed in [9]. Besides estimating phase and frequency, EPLL add amplitude loop in PLL scheme. After the three-phase signals are transformed into u_α and u_β are subtracted by the estimated components y_α and y_β to obtain the estimated errors e_α and e_β. Amplitude and frequency error are defined as

$$e_v = e_\alpha sin(\tilde{\theta}) + e_\beta sin(\tilde{\theta} - 90°) \tag{3}$$

$$e_w = e_\alpha cos(\tilde{\theta}) - e_\beta cos(\tilde{\theta} - 90°) \tag{4}$$

They are, respectively, integrated to obtain amplitude and passed to the PI controller for frequency estimation. By integrating $\tilde{\omega}$ estimated angle is obtained.

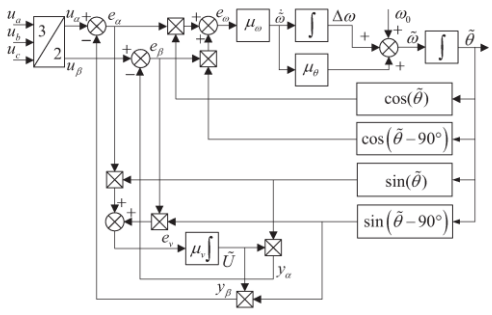

Fig. 4. Scheme of SF-EPLL [9]

D. DSOGI-PLL

Instead of filtering q component, DSOGI algorithm is designed in a way to prefilter $\alpha\beta$ components. Besides that, by dual integration, it is able to conserve information from positive sequenced harmonics by canceling negative sequenced harmonics in u'_α and u'_β by dividing with 2 voltage amplitude is preserved. Then u'_α and u'_β are transformed in dq components which further can be pass to standard SRF-PLL for frequency and phase estimation.

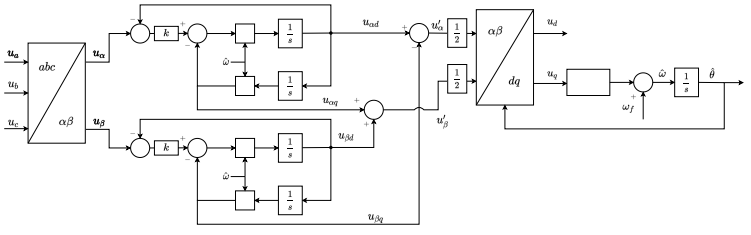

Fig. 5. Scheme of DSOGI-PLL

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IV. Selection of Parameters

A. SRF-PLL

Because of nonlinear structure of phase detector analysis and parameters selection would be complicated so model is linearized Fig. 6. From the obtained linear model, we can select parameters of PI controller to achieve desired response. Open loop transfer function is equal to:

$$W_{open}(s) = \frac{\varphi_{PLL}}{\varphi_{grid}} = \frac{sK_pK_{pd} + K_iK_{pd}}{s^2} \tag{5}$$

from which closed loop function is equal to:

$$W_{close}(s) = \frac{sK_pK_{pd} + K_iK_{pd}}{s^2 + sK_pK_{pd} + K_iK_{pd}} \tag{6}$$

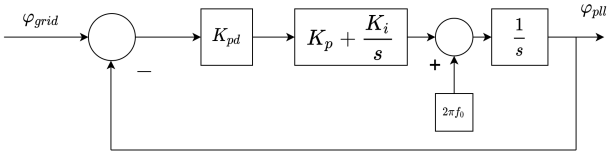

Fig. 6. Linearized model of SRF PLL

Where K_p, K_i are parameters of PI controller and Kpd represents amplitude of three-phase voltage. Selecting of parameters K_p and K_i is done to achieve desired bandwidth and damping by selecting coefficients to meet standard second order polynomial.

$$s^2 + 2\xi\omega_n s + \omega_n^2 = s^2 + sK_pK_{pd} + K_iK_{pd} \tag{7}$$

From where we can obtain parameters as:

$$K_i = \frac{\omega_n^2}{K_{pd}},\ K_p = \frac{2\xi\omega_n}{K_{pd}} \tag{8}$$

in this study, we chose $\xi = 1$ and $w_n = 37.7$ rad/s which corresponds with desired closed loop bandwidth of 6 Hz and absence of oscillations in response.

B. LAG-PLL

The idea of this PLL is to better filter higher harmonics than SRF. Since it only differs from SRF in added filter, we can use K_i and K_p used for SRF PLL. T_f is selected to minimize effect on system response. Open loop transfer function is equal to:

$$W_{open}(s) = \frac{\varphi_{PLL}}{\varphi_{grid}} = \frac{sK_pK_{pd} + K_iK_{pd}}{s^3T_f + s^2} \tag{9}$$

To find poles positions of closed loop in depending on T_f we used modified transfer function W_{mod}

$$W_{mod}(s) = \frac{T_f s^3}{s^2 + sK_pK_{pd} + K_iK_{pd}} \tag{10}$$

because closed loop poles for both transfer functions are the same. Poles position with respect to different value of T_f is shown in Fig. 7.T_f must be small enough to not interfere with system dynamics and large enough to filter higher harmonics. As a good compromise, T_f is selected to filter dynamics over 100Hz so $T_f = \frac{1}{200\pi}$.

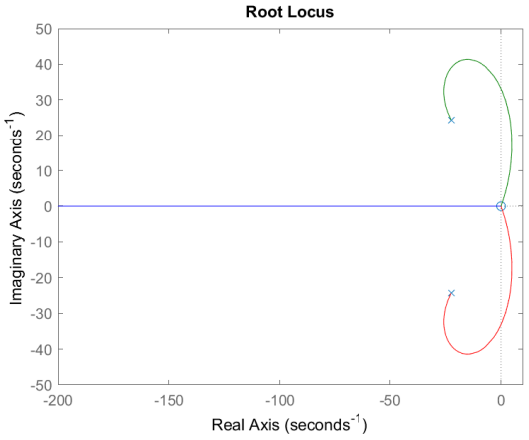

Fig. 7. Pole position for different values of T_f

C. DSOGI

Filtering power of dual integrator is determined by parameter, k which can we see in transfer functions from u_α to $u_{\alpha d}$ and u_α to $u_{\alpha q}$

$$G_d(s) = \frac{u_{\alpha d}}{u_\alpha} = \frac{k\omega_1 s}{s^2 + k\omega_1 s + \omega_1^2} \tag{11}$$

$$G_q(s) = \frac{u_{\alpha q}}{u_\alpha} = \frac{k\omega_1^2}{s^2 + k\omega_1 s + \omega_1^2} \tag{12}$$

transfer functions from u_β to $u_{\beta d}$ and u_β to $u_{\beta q}$ are the same.

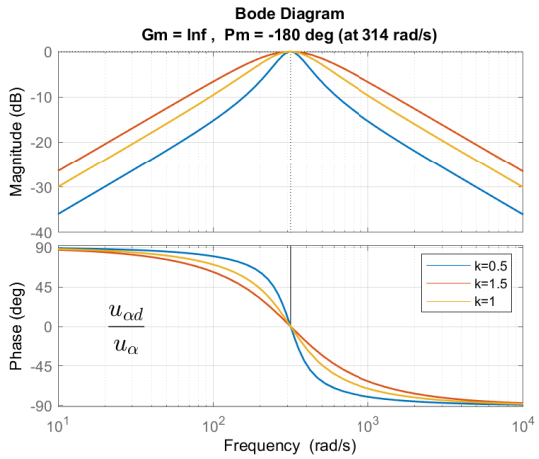

Fig. 8. Bode plot G_d in function of k

As it is shown on Fig. 8 and Fig. 9 increasing k give better attenuation of harmonics but also causes higher overshoot and greater settling time of estimation. For best trade-off $k = 1$ is selected. Parameters of PI controller K_i and K_p are same as in SRF and Lag-PLL.

D. SF-EPLL

For this PLL parameters for amplitude and frequency estimation can be chosen separately. For amplitude loop time

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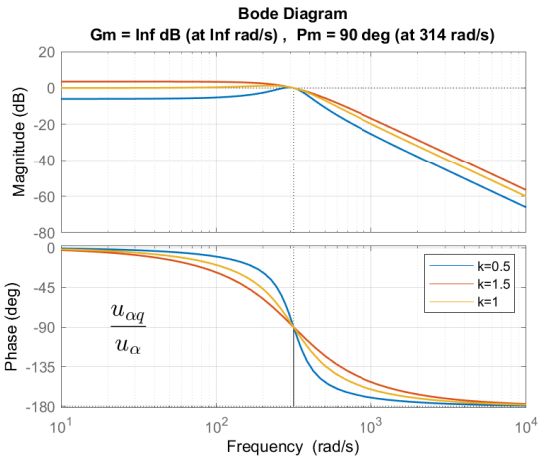

Fig. 9. Bode plot of G_q in function of k

constant of response is the same as $1/\mu_v$, from setting time of 50ms and $T_{sett} = 5/\mu_v$ we chose $\mu_v = 100$. Dynamic model of this PLL are provided in [9] from where $\mu_\theta = 2\xi/w_n$ and $\mu_\omega = w_n/\mu_\theta/U$ where U is estimate amplitude of grid voltage.

V. Simulation Results

Modeling of different PLLs and simulation is done by using Matlab and Simulink software.

Dynamic response of different PLLs is examined by step frequency change. As shown in Fig. 10 PLLs have similar rise time which means that regulation bandwidth is roughly the same. Despite, $\psi = 1$ overshoot is present due to the presence of dominant zero. Difference in overshoot is not crucial for performance of PLL.

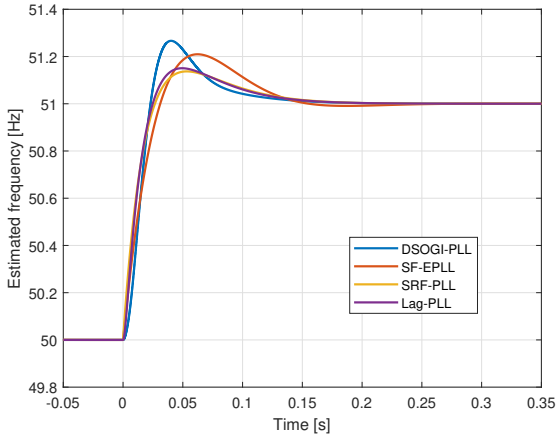

Fig. 10. Response on step frequency change

Unbalanced three-phase system is a problem for PLLs because it introduces ripple in frequency estimation. Unbalanced grid voltage used for simulation is shown in Fig. 11. Unbalanced grid conditions have the largest impact on SRF PLL. On the other hand, DSOGI is unaffected by distortions.

TABLE I
Performance comparison on step frequency change

PLL	Overshoot [%]	2% settling time [s]
SRF	13.70	0.143
Lag	15.05	0.140
SF-EPLL	20.95	0.138
DSOGI	26.65	0.130

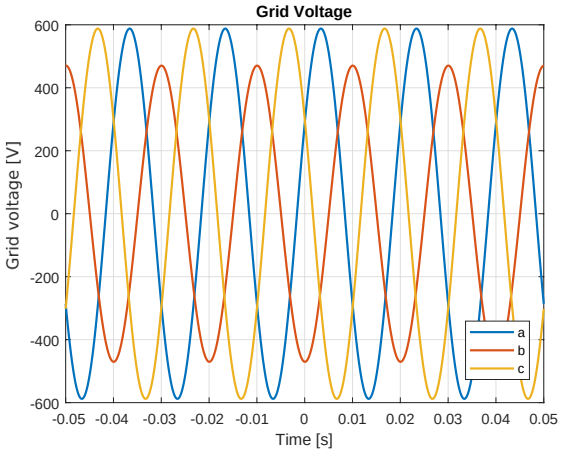

Fig. 11. Unbalanced grid voltage during simulation

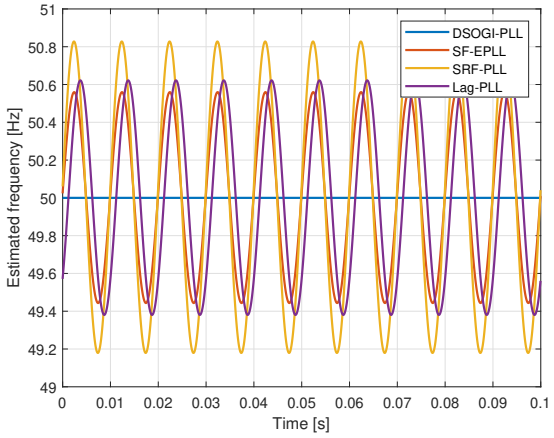

Fig. 12. Frequency estimation

TABLE II
Performance comparison in unbalanced conditions

PLL	Steady oscillation amplitude [Hz]
SRF	0.828
Lag	0.622
SF-EPLL	0.560
DSOGI	0

VI. Experimental Results

Experimental results were conducted of grid-connected inverter prototype. The prototype was designed for a grid with 208 V line voltage, so tests were conducted on that voltage. The algorithm is implemented on TMS320F28379D microcontroller. Experimental setup is shown on Fig. 13. The idea of this test is to show influence of real implementation

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and grid conditions on performance of PLL algorithms. Grid voltage with THD of 3.67% is shown on Fig. 14. Performance of different algorithms can be seen on Fig. 15 and Table III.

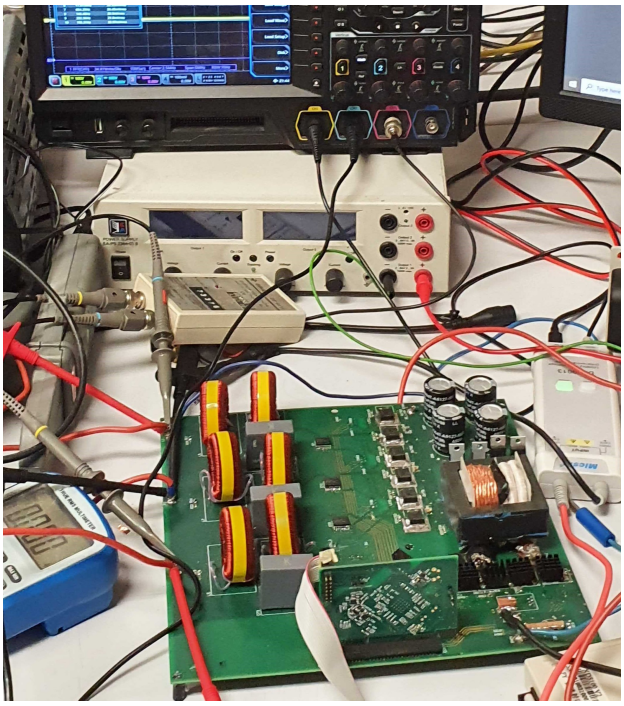

Fig. 13. Experimental setup

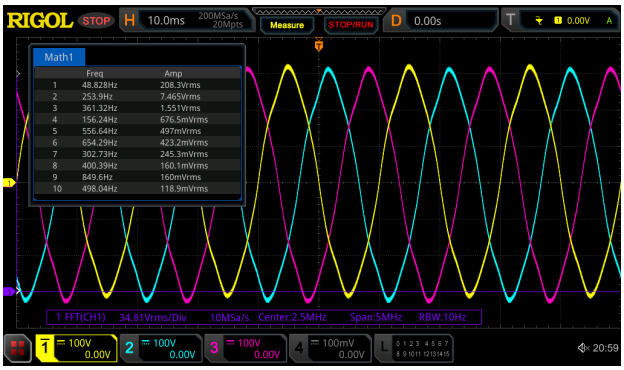

Fig. 14. Grid voltage

TABLE III
PERFORMANCE COMPARISON IN EXPERIMENTAL CONDITIONS

PLL	Maximum error [Hz]	Mean error [Hz]
SRF	0.771	0.439
Lag	0.675	0.4153
SF-EPLL	0.509	0.2930
DSOGI	0.357	0.224

VII. Conclusion

Analysis and performance comparison of four three-phase PLL structures have been simulated and tested on real prototype. From the presented comparison, it is found that DSOGI-PLL has the best performance in all three scenarios, providing the most accurate frequency estimation. Worst results are obtained with SRF-PLL which was expected knowing that all other PLLs presents modification of this algorithm in desire to achieve better performance. Future analysis will focus on quality of current injected to grid by inverter knowing the dynamic and performance of frequency estimation, which is essential for accurate grid synchronization.

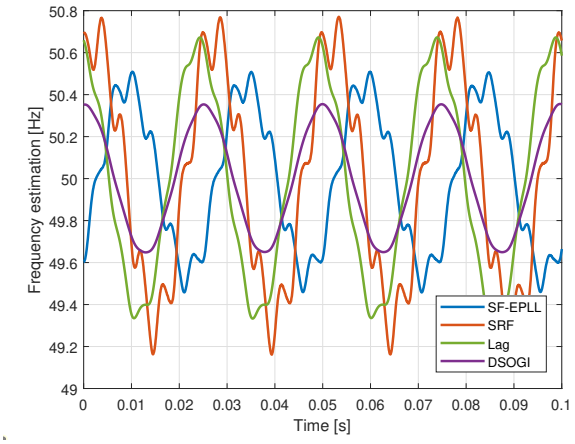

Fig. 15. Frequency estimation

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