Unified interfacing solution in video processing platforms based on FPGA

Marija Trifunović, Ilija Popadić, Vojislav Lukić, Miroslav Perić

***Abstract*—Video signal processing on various platforms is very common today, while the number of algorithms that use video signal as a source is still increasing. The problem occurs when the video signal from variety of cameras through various interfaces has to be imported to the platform for video processing. The usual approach is to use separate device that converts video signal from the source interface to the one that exists on the processing platform. The purpose of this paper is to describe various communication interfaces and propose the solution for their integration in the systems for video signal processing, with respect to the appropriate video standards. Detailed review of relevant standards is given. We propose the system, based on the last generation of FPGA device, including its model and implementation concept. This unified solution avoids the need for different converters and decrease the overall system price.**

***Index Terms*—FPGA, video signal, communication interfaces, conversion, Camera Link, 3G-SDI, HDMI, USB 3.0.**

I. Introduction

Video signal processing is very present in many new devices. There are a lot of modern architectures dedicated for this purpose and many manufacturers that implements these architectures into their own chips. Based on these chips, a number of platforms are developed with special purpose for video signal processing. Using these platforms performances of video signals processing are getting better. Manufacturers provide useful sources for developers in both hardware and software domain, which leads to the shorter time to the market.

For our research needs we had to prepare hardware setup that will be appropriate for general video processing algorithms evaluation such as video stabilization. Based on the existing experience we have chosen two powerful industrial platforms [1] [2] that are shown in the Fig 1.1. These platforms, in addition to existing communication interfaces, also have Universal Serial Bus (USB), Peripheral Component Interconnect Express (PCIe) and Gigabit Ethernet (GE). In order to achieve the full functionality of the setup, it was necessary to find suitable cameras and a way to connect them with a platform.

Exploring the industrial camera market leads to the conclusion that a lot of different communication interfaces are used. There is no unique communication interface even for cameras that use certain parts of the spectrum. For high definition video, which resolution exceeds 1 megapixel, the most commonly used interfaces are Camera Link (CL), Serial Digital Interface (SDI), GigE Vision, High-Definition Multimedia Interface (HDMI), CoaXPress (CXP), Camera Serial Interface (CSI). Using various interfaces introduces a problem of interfacing with the platform, since the only available are mentioned USB3.0, PCIe and Ethernet. Mentioned problem may be solved by using frame grabbers, devices that convert existing camera interface to those available on the chosen platforms.

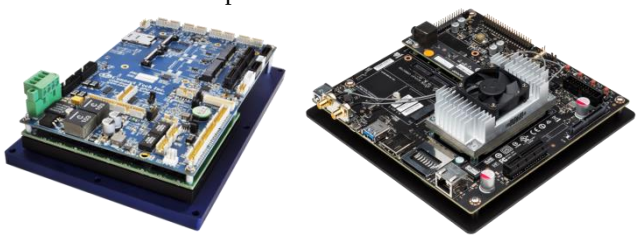

Figure 1.1. Evaluation platforms

During quality evaluation of cameras video signals, we have used two ways of interfacing, including USB and PCIe frame grabbers. We concluded that the most comfortable way for interfacing is to use USB frame grabber which has communication interface compatible with that one embedded in the camera. Block diagram of connecting camera with frame grabber and further with platform over available USB3.0 cable is shown in Fig. 1.2.

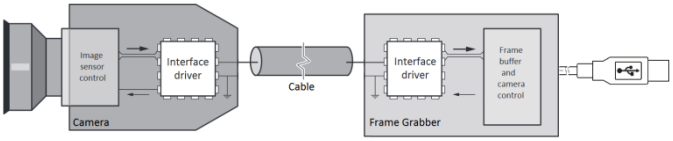

Figure 1.2. Connecting camera to the platform using frame grabber

Disadvantage of the mentioned principle for connecting a camera and a frame grabber is reflected in the fact that every communication interface requires a separate frame grabber. Also, there is no unified solution at the market that supports all interfaces in a single device. This is the main reason and

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motivation for the new solution development. This unified solution that supports most important communication interfaces in one device is based on the new generation of FPGA devices.

Prior to the implementation description in this paper, it is very important to understand all relevant communication interface terminology and standards in detail in order to choose appropriate solution possibilities and limitations. It is also necessary to be familiar with the newest dedicated hardware and software technologies available in the market for specific applications that are capable to support implementation of all chosen standards. After setting communication interface demands and selecting the appropriate platform it is possible to design the system model and continue with the description of system implementation.

II. CAMERA LINK INTERFACE

Camera Link is a serial communication protocol standard designed for computer vision applications based on the National Semiconductor interface Channel-link. It was launched in year 2000. as the first image processing standard and is currently the most popular interface for applications requiring very high resolutions and frame rates [3].

Camera Link operates on a point-to-point connection between camera and processing platform and requires a frame grabber. It is a hardware specification designed by camera and frame grabber manufacturers specifically for the needs of machine vision industry. It enables high speed data transfer between one or more cameras and frame grabbers. The data transmission rates of the Channel Link family chipsets (up to 2.38 Gbits/s) supports the current trend of increasing transfer speeds. It also provides mechanisms to control the cameras.

Camera Link uses one to three Channel link transceiver chips with four links at 7 serial bits each. Camera Link uses 28 bits to represent up to 24 bits of pixel data and 3 bits for video sync signals, leaving one spare bit. The video sync bits are Data Valid, Frame Valid, and Line Valid. Data is serialized 7:1, while the four data streams and a dedicated clock are driven over five Low-voltage differential signals (LVDS) pairs. The signal pendulum rate is 350 mV. Figure 2.1. illustrates Chanel link operation.

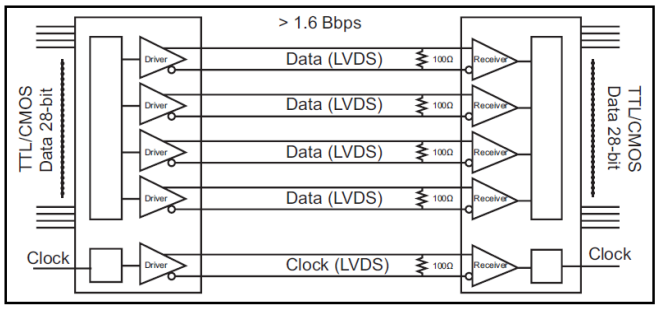

Figure 2.1. Chanel link operation [3].

Serial data rate has to be seven times higher than the clock frequency in order to accurately deserialize the serializable data. To ensure the highest accuracy, the interior of deserializer has a phase lock loop PLL, where the frequency produced by PLL clock is seven times of clock frequency. Clock relation is shown in Figure 2.2. [4].

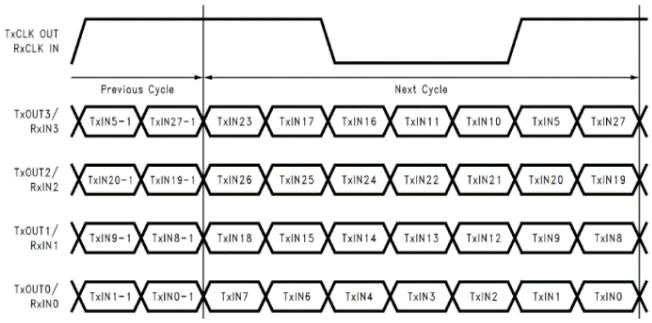

Figure 2.2. Clock relation of channel link [4].

The Camera Link standards includes five configurations. Each configuration supports a different number of data bits. Some of them require two cables for transmission. The five configurations are:

- Lite – supports up to 10 bits,
- Base – supports up to 24 bits,
- Medium – supports up to 48 bits,
- Full – supports up to 64 bits,
- 80 bits – supports up to 80 bits.

The first two configurations require one connector, and the other three require two connectors.

Four enable signals for Camera Link Base/Medium/Full are defined as [3].

- FVAL – Frame Valid is defined High for valid lines, and envelopes all lines in frame
- LVAL – Line Valid is defined High for valid pixels, and envelopes all pixels in line,
- DVAL – Data Valid is defined high when data is valid, and qualifies valid pixels in a line,
- Spare – A spare has been defined for future use.

All defined enables must be provided by the camera on each Channel Link chip. All unused data must be tied to a known value by the camera.

The 80-bit configuration uses some of the signals to carry enable for data, and the spares are also used for data, so the enables lines are only FVAL and LVAL, as defined above.

Camera link interface has two ports, camera, and frame grabber. Camera link interface structure is: three camera link interfaces with the direction from Camera to Frame Grabber, used for image data transmission, and a four-channel camera control interface with the direction from Frame Graber to Camera, usually used for camera exposure trigger control. Two LVDS pairs have been allocated for asynchronous serial communication to and from the camera and frame grabber. Camera and frame grabber should support at least 9600 baud [3].These signals are:

- SerTFG – Differential pair with serial communications to the frame grabber
- SerTC – Differential pair with serial communication to camera.

Camera link interface is shown in Figure 2.3.

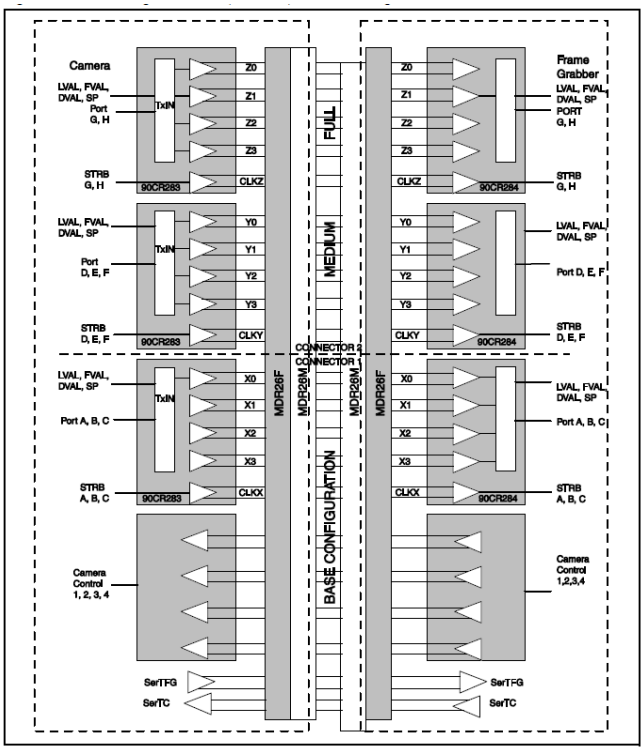

Figure 2.3. Camera link interface structure [3]

III. SERIAL DIGITAL INTERFACE

Serial digital interface (SDI) is a digital video interface for transmission over coaxial cable, standardized by SMPTE in 1989. ITU-R BT.656 [5] and SMPTE 259M [6] define digital video interfaces used for broadcast grade video. Additional SDI standards have been introduced to support increasing video resolutions frame rates, stereoscopic video, and color depth. 3G-SDI standardized in SMPTE 424M consists of a single 2.970 Gbit/s serial link that allows replacing dual link HD-SDI [7]. 6G-SDI [8] and 12G-SDI [9] standards were published in 2015. These standards are used for transmission of uncompressed, unencrypted digital video signals within television facilities along with embedded ancillary data such as multiple audio channels. Standard 75-ohm cable is used for transmission [10].

Regular television video display resolutions are referred by their vertical resolution such as 1080p or 1080i, where *p* stands for progressive, *i* stands for interlaced, and 1080 refers to the number of vertical pixels. Digital cinema display resolutions are referred by their horizontal resolution [11]. 1080p also known as HDTV 2K is the term used for television display resolution where 2K is the corresponding to a cinema resolution (due to the 2048 horizontal pixels [12].

Video frames are stored as either RGB or YCbCr color sequences. In RGB model, R stands for Red, G for green and B for the Blue component. In the YCbCr, Y refers to the luma component, while Cb refers to the chrominance component of the blue color and Cr to the chrominance component of the red color.

The SMPTE 424 and SMPTE 425 [13] are a family of standards that describe the transport and mapping of 3G-SDI video mode and how ancillary data should accompany video in a 3G signal data interface. The transport of 3G-SDI video mode comprises a set of video formats that can fit to 2.97Gbps. It can be presented as an uncompressed video container and electrical standard at the same time. The transport of video is made frame by frame, being that each frame is transmitted line by line serially. Every full line of video pixel information is accompanied by some dedicated space for ancillary data. That is called the Horizontal Ancillary video space (HANC). Active Video area and HANC are sent through the same stream, so there is the need of sending video line starts (SAV) and ends (EAV) flags. Ancillary data can also be sent through Vertical Ancillary data space, called VANC. Figure 3.1. shows how video data is transported according SMPTE 424 standard [7].

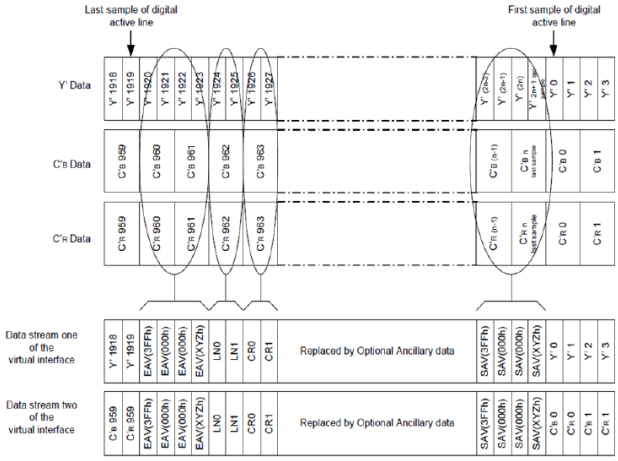

Figure 3.1. Mapping structure 4:2:2 (Y'Cb'Cr')/10 bit signals [7]

External SDI cable equalizers and cable drivers are required to convert the serial signals into the receiver and out of the transmitter according to the SDI electrical standards. An external SDI cable equalizer must be used to convert the single-ended 75-ohm SDI signal to a 50-ohm differential signal compatible with the receiver input signal requirements.

IV. HIGH DEFINITION MULTIMEDIA INTERFACE - HDMI

High definition multimedia interface is audio and video interface for transmitting uncompressed video data and compressed or uncompressed digital audio data from a HDMI compliant source device, such as a display controller, to a compatible device. HDMI implements the EIA/CEA-861 standards [14], which define video formats and waveforms, transport of compressed, uncompressed, and LPCM audio, auxiliary data, and implementations of the VESA EDID.

HDMI link includes three Transition minimized Differential Signaling-TMDS Data channel and a single TMDS Clock channel. Clock channel runs at a rate proportional to the pixel rate of the transmitted video. During every cycle of the clock, each of the three TMDS data channels transmits a 10-bit character.

These data items are processed in a variety of ways and are presented to the TMDS encoder as either 2 bits of control data, 4 bits of packet data or 8 bits of video data per TMDS channel. The source encodes one of these data types or encodes a Guard Band character on any given clock cycle. Figure 4.1. shows block diagram of HDMI encoder and Decoder.

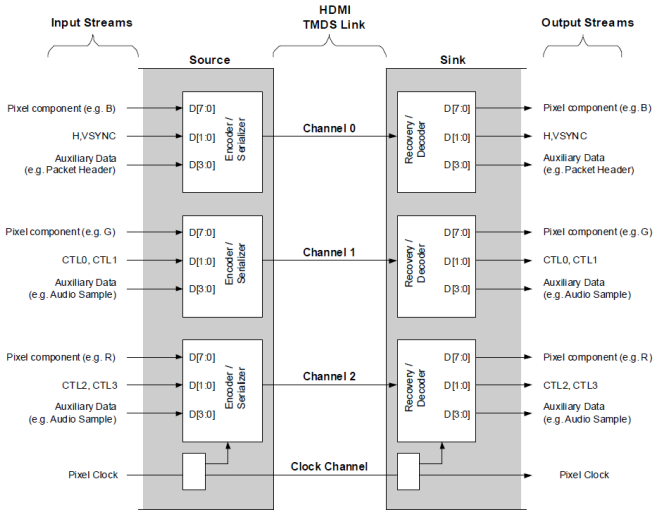

Figure 4.1. HDMI encoder/decoder [15]

The HDMI link operates in one of three modes: video data period, data island period, and control period. Audio and auxiliary data are transmitted in data island period. Control period is necessary between any two periods that are not control periods. Video data periods use transition minimized coding to encode 8 bits per channel, or 24 bits total per pixel. Data island period are encoded using a similar transition minimized coding, TMDS error reduction coding TERC4, that transmits 4 bits per channel or 12 bits per clock period [16].

HDMI devices are developed according various versions of the specification, in which each version is given a number or letter, such as 1.0, 1.2, or 1.4b. Each subsequent version of the specification uses the same kind of cable but increases the bandwidth or capabilities of what can be transmitted over the cable.

V. Universal Serial Bus Interface- USB

Universal Serial Bus is an industry standard that intended to be used as one of the dominant communication protocol for serial data exchange between devices. This standard was designed to be an effective substitute for data transfer by conventional communication ports at PC machine such as RS-232 and parallel port. USB specification defines almost all details ranging from mechanical connectors and cables, the principles of operation interface, data transmission on the network level, and power management devices that connect to the USB interface.

The USB consists of a host and its devices, which are connected in a hierarchical star topology. USB standard is not intended to transfer clock signal, so that communication is asynchronous. Transmitted data by road are encoded using NRZI (non-return-to-zero-inverted) code with the additional use of techniques for inserting bits (bit stuffing) [17].

Basic communication unit for transmitting data messages is USB's package. The package consists of the three parts:

- Start
- Information packet
- The end of the packet identifier - EOP

Start represents the transition from the idle state that is passive condition, into an active state. Active state is defined by changing the polarity. Beginning of the packet sequence transition is called SYNC.

Information packet has the length from 1 bit to 1024 bits. This section consists of a Packet Identifier (PID) and useful information (payload).

During EOP period the both lines are set to low for a period of two bit-intervals. High speed bus EOP takes 40-bit interval with no transition.

A predefined sequence of packets is referred to as the transfer. USB standards specify the 4 different types of transfer that are designed to copy different types of data [17]:

- Control transfer type - non-periodic transfer mainly used for transfer of control and status information,
- Isochronous transfer - this type is used for streaming data such as video. This type of transmission is error tolerant and is only supported by the high-speed devices,
- Interrupt - periodic type with a guaranteed latency of transfer between the transaction.
- Bulk transfer - not a periodic transfer, mainly used to transfer large amounts of data

USB 3.0 is the second major revision of the Universal Serial Bus standard for computer connectivity. USB 3.0 implements a 5.0 Gbit/s raw transfer rate using 8b/10b encoding. USB 2.0 implements the Hi-Speed mode HS with bit rate 480 Mbit/s, while USB 1.1 implements Low Speed (LS) with bit rate 1.5 Mbit/s and Full Speed (FS) with bit rate 12 Mbit/s. [18].

VI. FPGA Implementation

Import of video signal on different video platforms is done using dedicated hardware and multiple software tools, generally speaking. To achieve real time high-performance video signal interface conversion, it is needed that system supports the functioning and conversion without frame losses. This requires the use of several Intellectual Property (IP) Cores and compatibility with a wide set of standards [12].

Field Programmable Gate Arrays (FPGA) are designed to be configured after production. This corresponds to the most flexible hardware configurable platform available in the field. In this application, FPGA is used for hardware implementation of unique interfacing solution for conversion between different video data interface inputs to the USB interface output.

This system is complex and requires multiple hardware description HDL blocks as well as the assembly of IP cores.

Unlike the other system available in the market, this application is capable to accept video signals from camera with different interface outputs, and convert them to the unique output interface in order to connect them to the video platform for further processing. Supported interface conversions in the system are shown in Figure 6.1.

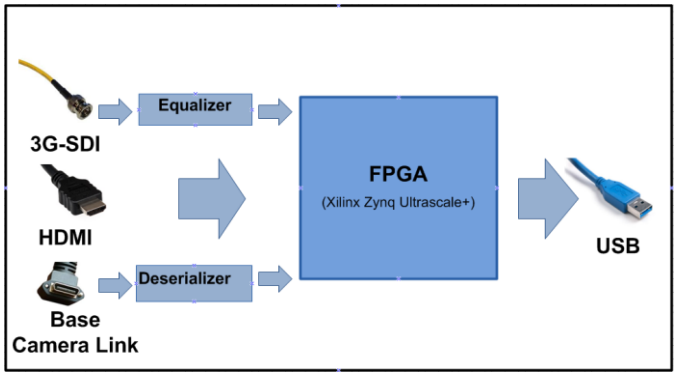

Figure 6.1. Interface conversions in the system

There are three types of camera interface that are supported by this system. Video signal can be imported to the FPGA platform through either 3G-SDI, HDMI, or Base Camera Link interface. System automatically recognizes the type of the interface depending on camera that is connected and converts the input stream format into USB 3.0 interface format for further connection to the video processing platform.

In our soulution Xilinx Zynq UltraScale+ XCZU9EG-2FFVB1156 FPGA chip is used. Xilinx provides a wide range of transceivers and supporting IP cores for different types of applications from low-cost consumer products to high-end networking systems. Xilinx transceivers cover the scale of high speed protocols available on the market. This specific chip has 4 GTR transceivers that supports up to 6Gbit/s bit rate, and allows easiest integration of common protocols to the Zynq Processor Subsystem. It also has 24 GTH transceivers that support bit rate up to 16.3 Gb/s, and allows implementation of all supported interfaces by this application. Figure 6.2. shows block diagram of the conversion platform.

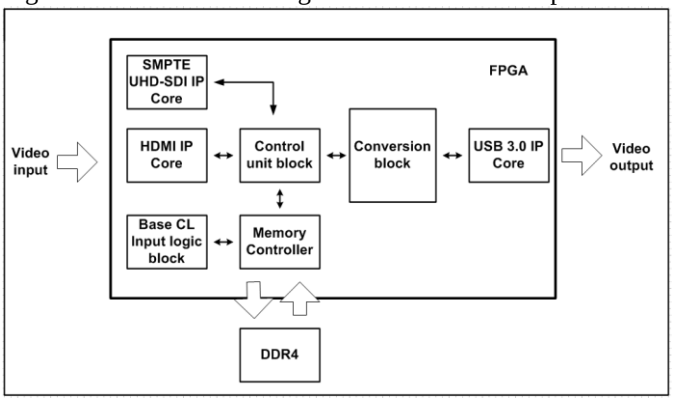

Figure 6.2. Block diagram of the FPGA system

The implementation of 3G-SDI is done using Xilinx SMPTE UHD-SDI IP core. It is connected to a GTH transceiver. The core is capable of supporting SMPTE SD-SDI, HD-SDI, 3G-SDI, 6G-SDI and 12G-SDI standards [19], but applications is limited by the output side, USB 3.0 interface, that can support only up to 5 Gb/s. This application supports transmission of HDTV (1080p) at 4:2:2, 10 bit, video format through a single SDI cable. The 1080p format is composed of frames with the resolution of 1080 vertical pixels by 1920 horizontal pixels. This means that every video line is made of 1920 pixels from a total of 1080 video lines. Each pixel is represented by 10 bits at 4:2:2, which means 38,400 bits per line. Appropriate SDI cable equalizers are available from several manufacturers. For our application, we have chosen Semtech GS6042 cable equalizer, and Semtech GS6080 cable driver for the loopback test.

This application supports HDMI 1.4. standard that provides the maximum resolution of 4K×2K. The implementation of HDMI interface is done using HDMI 1.4/2.0 Receiver Subsystem IP core. It is a hierarchical IP that bundles a collection of HDMI RX IP sub-cores and outputs them as a single IP [20].

For the implementation of Camera Link interface there was no need for usage of Xilinx IP core, because the signal was converted through the National Semiconductor DS90CR288A receiver deserializer chip that supports clock rates from 20 MHz to 85 MHz. Twisted pair for communication between the camera and the frame grabber are implemented using National Semiconductor DS92LV1021A 10-bit Serializer. For the testing purpose, we have used National Semiconductor DS90CR287 LVDS 28-bit transmitter chip in the loopback test that supports the same clock rates as receiver. The custom HDL code was implemented for the management of the input signal. Our application supports only the Base Camera link configuration, which means that only one connector is required per channel side.

The implementation of USB 3.0 interface is done using A USB 3.0 Device IP Core that provides high performance SuperSpeed USB connectivity. Used USB 3.0 controller shall provide one 5.0Gbit/s USB channel using the internal Processing subsystems (PS) Gigabit Transfer (GT) as physical layer (PHY).

VII. Conclusion

Implementation has proved that this unified interfacing solution has a lot of advantages in comparison with existing ones available at the market. First of all, there is no need for several interfacing boards, one per every interface. Also, it is highly configurable and may be adopted if some camera interface has its own customization. There should be highlighted that during this development process we have achieved high knowledge skills about camera communication interfaces, specific cables and connector types that should be used.

In our further research and development, we plan to extend current system in a way that it could support even higher speed interfaces, such as 6G-SDI and 12G-SDI, by implementing PCIe for the output interface, and adopt current

system design to the new requirements.

REFERENCES

[1] "http://connecttech.com/product/com-express-gpu-embedded-system/," Connect Tech Inc, 2016. [Online].

[2] "https://developer.nvidia.com/embedded/buy/jetson-tx1-devkit," Nvidia Corporation, 2016. [Online].

[3] "Specifications of the Camera Link Interface Standard for Digital Cameras and Frame Grabbers, version 2.0.," Automated Imaging Association, Ann Arbor, 2012.

[4] W. Gang, L. Cai, W. Shigang,, G. Kai and W. Xiaolan, "Implementation of Camera Link Interface on Virtex-5 FPGA," *Research Journal of Applied Sciences, Engineering and Technology*, pp. 5244-5248, 2013.

[5] "ITU-R Recommendation BT.656,Interfaces for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601 (Part A)," International Telecommunication Union, 2007.

[6] "SMPTE 259M- SDTV Digital Signal/Data Serial Digital Interface," ANSI/SMPTE, 2008.

[7] "SMPTE 424M - 3 Gb/s Signal/Data Serial Interface," ANSI/SMPTE, 2006.

[8] "SMPTE ST 2081-10: 2160 line and 1080 line source image and Ancillary Data Mapping for Single Link 6G-SDI," SMPTE, 2015.

[9] "SMPTE ST 2082-10: 2160-line Source Image and Ancillary Data Mapping for 12G-SDI," SMPTE, 2015.

[10] C. Poynton, Digital Video and HDTV Algorithms and Interfaces, Morgan Kaufmann Publishers, 2003.

[12] J. R. S. d. Sá, PhD Disertation: Study on the FPGA implementation of the conversion of uncompressed High-Definition video signals for distribution over IP networks, Faculdade de Engenharia da Universidade do Porto, 2016.

[13] "SMPTE 425-1- Source Image Format and Ancillary Data Mapping for the 3 Gb/s Serial Interface," SMPTE, 2014.

[14] "CEA-861-D, A DTV Profile for Uncompressed High Speed Digital Interfaces".

[15] "High-Definition multimedia interface, Specification Version 1.4," HDMI Licensing, LLC, 2009.

[16] "High-Definition Multimedia Interface Specification 1.3a," HDMI Licensing, LLC., November 10, 2006. Retrieved April 1, 2016.

[17] "Universal Serial Bus 3.1 Specification," Hewlett-Packard Company, Intel Corporation, Microsoft Corporation, Renesas Corporation, ST-Ericsson, and Texas Instruments, 2013.

[18] "http://www.wiki.xilinx.com/Zynq+Ultrascale+MPSOC+Linux+USB+device+
driver," Xilinx, 2016. [Online].

[19] Implementing SMPTE SDI Interfaces with UltraScale GTH Transceivers, 2016: Xilinx.

[20] HDMI 1.4/2.0 Receiver Subsystem v2.0 Product Guide, Xilinx, 2017.

[21] N. Li-pi, J. Xiu-hua, S. Dong-xin and Z. Wen-hui, "Design and implementation of SDI based on FPGA," in *International Conference on Networking and Information Technology*, Beijing,China, 2010.