Worst Case Start-up Estimation of the Half Wave Capacitive Divider Power Supply

Vladimir Rajović, Nenad Jovičić and Aleksandra Lekić

Abstract—Analysis of start-up transient of Half Wave Capacitive Divider Power Supply is presented, for entire range of initial phase. Duration of start-up transient is estimated, and approximate formula for its higher boundary is developed.

Index Terms—AC-DC power conversion; capacitive divider power supply; approximate formulas; start-up transient.

I. INTRODUCTION

THE basic half wave capacitive divider power supply (HWCDPS) circuit presents small, lightweight and low cost circuit. It is shown in Fig. 1, where the circuit load is represented by a constant current sink. HWCDPS is used for low power AC-DC voltage conversion. Although the circuit is not isolated, there are numerous fields of its application: practically all user-interface-less, mains powered, low power devices or subsystems in an electric or electronics device.

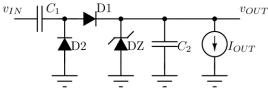


Fig. 1. The basic HWCDPS.

Capacitive divider power supplies (CDPS) seem to be considered a part of common electric engineering legacy. CDPS are not mentioned in power electronics monographs [1-2], although they are widely used. There are only a few application notes discussing the design of HWCDPS [3]– [5], but none of them took into consideration the startup transient of the circuit. A quantitative analysis of the HWCDPS during the start-up and after reaching the steadystate, with the assumption of ideal circuit components and turn-on at the mains zero crossing, is given in [6].

In short, in the steady state the output voltage of the circuit varies between v_{OUTmax} and v_{OUTmin} , at the frequency f = 1/T of the input voltage $v_{IN} = V_m \sin(2\pi ft)$. In the first approximation, the output voltage increases and decreases simultaneously with the input voltage. The Zener diode limits the output voltage at $V_Z = v_{OUTmax}$, thus dissipating any surplus input power. A larger output capacitance C_2 decreases the output voltage ripple whereas a larger input capacitance C_1 increases the available output current and shortens the time needed for the circuit to enter steady-state after power-on. If the increase of the output

capacitance C_2 is not accompanied with a corresponding increase of the input capacitance C_1 , the circuit may be prevented from entering the steady-state.

In this paper, we estimate the time interval between the circuit turn-on and the moment when the Zener diode in the circuit breaks down for the first time, marking the entrance of the circuit into the steady-state operation. This time interval represents the HWCDPS start-up time and is an important feature of the circuit, that could be traded-off for the output voltage ripple and power dissipation of the circuit.

II. TURN-ON OPERATION OF THE HWCDPS

The HWCDPS operates without reaching the steady-state for some time after turn-on. That is, there is a time interval during which the output voltage doesn't reach Zener diode DZ breakdown voltage, thus the diode DZ doesn't conduct. During that time interval, the local maximums of the output voltage increase gradually. Typical input and output voltage waveforms during the start-up period are shown in Fig. 2 for various turn-on time instants relative to the mains. The meanings of the symbols in Fig. 2 are as follows: τ_{2j} are the time instants the series diode D1 turns on, when the output voltage has local minimums; τ_{2j+1} are the time instants the series D1 diode turns off, when the output voltage has local maximums; *j* is the ordinal number of the input voltage cycle counting from zero; Θ is the time instant the Zener diode DZ breaks down for the first time. The ordinal number of input voltage cycle the circuit enters steady state at can be estimated as k = 1 + j, so $\tau_{2j+1} > \Theta > \tau_{2j}$. As illustrated in Fig. 2a and Fig. 2d, there is a degree of uncertainty about exact moment the breakage occurs, but it can be bounded by $\pm \pi / 2\omega$ around the start of the kth cycle of the input voltage. One cycle of the operation during the circuit's start-up consists of four subcycles. In the first subcycle, the input voltage v_{IN} increases, the series diode D1 conducts and the output capacitor is being charged. In the remaining three subcycles the output capacitor is being discharged through the current sink I_{OUT} . In the second subcycle the input voltage decreases, and both series diode D1 and parallel diode D2 are turned off. In the third subcycle the input voltage decreases, the series diode is turned off, and the parallel diode conducts. In the fourth subcycle the input voltage increases, and both series and parallel diode are turned off.

In the analysis, we use the symbols from Fig. 2. and assume ideal diodes with zero forward voltage drop as well as the ideal Zener diode with the breakdown voltage V_Z , and the load modeled as a constant current sink I_{OUT} .

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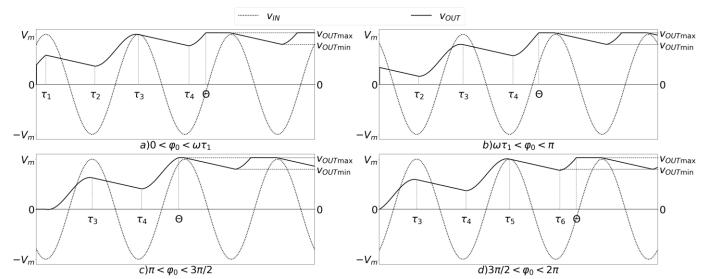


Fig. 2. Typical output voltage v_{OUT} waveforms of HWCDPS during start-up period for various initial phase φ_0 of the input voltage v_{IN} .

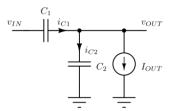


Fig. 3. Equivalent circuit of HWCDPS when only series diode conducts.

Let us consider the transition between the first and the second subcycle, that is, the time instant τ_{2j+1} . The equivalent circuit is shown in the Fig. 3. The value of the output voltage for $t = \tau_{2j+1}$ is [6]:

$$v_{OUT}(\tau_{2j+1}) = v_{OUT}(\tau_{2j}) + \frac{C_1}{C_1 + C_2} V_m \left(\sin \omega \tau_{2j+1} - \sin \omega \tau_{2j}\right) - \frac{I_{OUT}}{C_1 + C_2} (\tau_{2j+1} - \tau_{2j})$$
(1)

and it represents a local maximum. The moment τ_{2j+1} can be exactly determined [6]:

$$\tau_{2j+1} = \frac{1}{\omega} \left(\arccos\left(-\frac{I_{OUT}}{C_2 V_m \omega} \right) + 2j\pi \right) = \tau_1 + \frac{2j\pi}{\omega}, \quad (2)$$

where τ_1 denotes the very first moment the series diode turns off as can be seen in the Fig. 2a. Depending on the initial phase of the input voltage, τ_1 may not actually be in accord with (2). In cases when it doesn't match the equation (2), we would formally use τ_3 as the time of the first regular output voltage maximum, see Figs. 2b-d. From the moment τ_{2j+1} on the output voltage linearly decreases.

Let's now consider the transition between the fourth and the first subcycle, that is τ_{2j} . The equivalent circuit is shown in the Fig. 4. The input capacitor C_1 is charged at $-V_m$, and the diode D1 turns on when [6]

$$V_m(\sin \omega \tau_{2j} + 1) = v_{OUT}(\tau_{2j-1}) - \frac{I_{OUT}}{C_2}(\tau_{2j} - \tau_{2j-1})$$
(3)

The output voltage is then [6]

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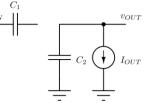


Fig. 4. Equivalent circuit of HWCDPS when no diode conducts.

$$v_{OUT}(\tau_{2j}) = v_{OUT}(\tau_{2j-1}) - \frac{I_{OUT}}{C_2}(\tau_{2j} - \tau_{2j-1}). \quad (4)$$

In order to obtain the ordinal number of the input voltage cycle when the Zener diode first starts conducting in the breakdown (accounting for a possible incomplete first cycle due to stochastic nature of the initial phase), equations (1)-(4) are solved. From equation (2), τ_{2j+1} and $\sin \omega \tau_{2j+1}$ are obtained: $\tau_{2j+1} = \tau_{2j-1} + 2\pi / \omega$, $\sin \omega \tau_{2j+1} = \sin \omega \tau_1$ and substituted in (1) along with (4)

$$v_{OUT}(\tau_{2j+1}) = v_{OUT}(\tau_{2j-1}) + \frac{C_1}{C_1 + C_2} V_m \sin \omega \tau_1 - \frac{C_1}{C_1 + C_2} \left(V_m \sin \omega \tau_{2j} + \frac{I_{OUT}}{C_2} (\tau_{2j} - \tau_{2j-1}) \right) - \frac{I_{OUT}}{C_1 + C_2} \frac{2\pi}{\omega}.$$
(5)

Rearrangement of (3) yields

$$\frac{I_{OUT}}{C_2} \left(\tau_{2j} - \tau_{2j-1} \right) + V_m \sin \omega \tau_{2j} = v_{OUT} \left(\tau_{2j-1} \right) - V_m,$$

that is substituted in (5):

$$v_{OUT}(\tau_{2j+1}) = \frac{C_2}{C_1 + C_2} v_{OUT}(\tau_{2j-1}) + \frac{C_1}{C_1 + C_2} V_m \sin \omega \tau_1 + \frac{C_1}{C_1 + C_2} \left(V_m - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_1} \right).$$
(6)

If we substitute j with j - 1 in (6) there is

$$v_{OUT}(\tau_{2j-1}) = \frac{C_2}{C_1 + C_2} v_{OUT}(\tau_{2j-3}) + \frac{C_1}{C_1 + C_2} V_m \sin \omega \tau_1 + \frac{C_1}{C_1 + C_2} \left(V_m - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_1} \right).$$
(7)

Equations (6) and (7) provide expression

$$v_{OUT}(\tau_{2j+1}) = \left(\frac{C_2}{C_1 + C_2}\right)^2 v_{OUT}(\tau_{2j-3}) + \left(1 + \frac{C_2}{C_1 + C_2}\right) \frac{C_1}{C_1 + C_2} V_m \sin \omega \tau_{2j}$$
$$+ \left(1 + \frac{C_2}{C_1 + C_2}\right) \frac{C_1}{C_1 + C_2} \left(V_m - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_1}\right).$$
(8)

If *j* is substituted with j - 1 in (7), there is expression

$$v_{OUT}(\tau_{2j-3}) = \frac{C_2}{C_1 + C_2} v_{OUT}(\tau_{2j-5}) + \frac{C_1}{C_1 + C_2} V_m \sin \omega \tau_1 + \frac{C_1}{C_1 + C_2} \left(V_m - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_1} \right),$$
(9)

that, with equation (8), gives:

$$v_{OUT}\left(\tau_{2j+1}\right) = \left(\frac{C_2}{C_1 + C_2}\right)^3 v_{OUT}\left(\tau_{2j-5}\right)$$
$$+ \frac{C_1}{C_1 + C_2} \left(V_m\left(1 + \sin \omega \tau_1\right) - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_1}\right) \sum_{i=0}^2 \left(\frac{C_2}{C_1 + C_2}\right)^i.$$

Similarly, it can be determined

$$v_{OUT}(\tau_{2j+1}) = \left(\frac{C_2}{C_1 + C_2}\right)^4 v_{OUT}(\tau_{2j-7}) + \frac{C_1}{C_1 + C_2} \left(V_m(1 + \sin \omega \tau_1) - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_1}\right) \sum_{i=0}^3 \left(\frac{C_2}{C_1 + C_2}\right)^i$$

and further iterations developed. From the previous analysis, the output voltage at $t = \tau_{2j+1}$ is determined:

$$v_{OUT}(\tau_{2j+1}) = \left(\frac{C_2}{C_1 + C_2}\right)^p v_{OUT}(\tau_{2j+1-2p}) + \frac{C_1}{C_1 + C_2} \left(V_m(1 + \sin \omega \tau_1) - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_1}\right) \sum_{i=0}^{p-1} \left(\frac{C_2}{C_1 + C_2}\right)^i$$
(10)

If we substitute 2j + 1 - 2p = 1, that is p = j, in (10), and apply the identity $\sum_{i=0}^{j} x^{i} = \frac{1 - x^{j}}{1 - x}$, the relation of the $(j + 1)^{\text{th}}$

and the first local maximum of the output voltage when the Zener diode DZ does not break down is

$$v_{OUT}\left(\tau_{2j+1}\right) = \left(\frac{C_2}{C_1 + C_2}\right)^j v_{OUT}\left(\tau_1\right) + \left(1 - \left(\frac{C_2}{C_1 + C_2}\right)^j\right) \left(V_m\left(1 + \sin\omega\tau_1\right) - \frac{2\pi}{\omega}\frac{I_{OUT}}{C_1}\right)$$

Another substitution j + 1 = k yields a more concise expression for the k^{th} (occurring during the k^{th} cycle of the input voltage) local maximum of the output voltage during start-up of the HWCDPS

$$v_{OUT \max}\left(k\right) = \left(\frac{C_2}{C_1 + C_2}\right)^{k-1} v_{OUT \max}\left(1\right)$$

$$+ \left(1 - \left(\frac{C_2}{C_1 + C_2}\right)^{k-1}\right) \left(V_m \left(1 + \sin \omega \tau_1\right) - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_1}\right)$$
(11)

Start-up transient ends and the circuit enters steady-state τ_1 during the k^{th} cycle of input voltage, when (and if)

$$v_{OUT\max}(k) \ge V_Z. \tag{12}$$

As can be seen from Fig. 2., $v_{OUT(max)}(1)$, that is $v_{OUT}(\tau_1)$, depends on φ_0 , the phase of the input voltage at the initial time instant. Before proceeding, we will assume initially discharged capacitors, $C_1 << C_2$, and introduce some additional approximations:

$$\frac{I_{OUT}}{C_2 V_m \omega} \ll 1 \Longrightarrow \sin \omega \tau_1 \approx 1, \, \omega \tau_1 \approx \frac{\pi}{2}$$
(13)

$$\left(\frac{C_2}{C_1 + C_2}\right)^n \approx 1 - n \frac{C_1}{C_1 + C_2}.$$
 (14)

After application of (13) and (14) to (11) and substitution, (12) becomes

$$V_{Z} \ge \left(1 - (k - 1)\frac{C_{1}}{C_{2}}\right) v_{OUT \max}(1) + (k - 1)\frac{C_{1}}{C_{2}} \left(2V_{m} - \frac{2\pi}{\omega}\frac{I_{OUT}}{C_{1}}\right)$$
(15)

In some cases, this local maximum is irregular, that is it occurs at $t > \tau_1$ (as seen in Figs. 2b-d), and (15) should be changed accordingly

$$V_{Z} \ge \left(1 - (k - 2)\frac{C_{1}}{C_{2}}\right) v_{OUT \max}(2) + (k - 2)\frac{C_{1}}{C_{2}} \left(2V_{m} - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_{1}}\right)$$
(16)

We can evaluate if the circuit would ever enter steady state, that is if the Zener diode breaks down for given capacitances C_1 and C_2 . Should there be no Zener diode in the circuit, the maximum output voltage is, from (11) and for $k \rightarrow \infty$:

$$v_{OUT\max}\left(\infty\right) = V_m\left(1 + \sin\omega\tau_1\right) - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_1} \approx 2V_m - \frac{2\pi}{\omega} \frac{I_{OUT}}{C_1}$$
(17)

In order the Zener diode to break down, it should be $v_{OUTmax}(\infty) > V_Z$, that is:

$$C_1 > \frac{2\pi}{\omega} \frac{I_{OUT}}{2V_m - V_Z} \tag{18}$$

The result (18) provides information about the minimum series capacitance C_1 , for given V_Z and I_{OUT} , in order to ensure circuit steady-state operation.

The ordinal number of the input voltage cycle when Zener diode breaks down for the first time (the measure of the HWCDPS start-up time) is estimated next. There are four possible cases, depending on the initial phase of the input voltage.

A. Input voltage phase is $0 \le \varphi_0 \le \omega \tau_1$

At the circuit turn-on, there is an irregular commutation at the capacitors C_1 and C_2 through the diode D1, so the output voltage leaps to

$$v_{OUT}\left(\tau_{0}\right) = \frac{C_{1}}{C_{1}+C_{2}}V_{m}\sin\varphi_{0}.$$

Afterwards, the diode D1 conducts and the output voltage rises up to the first local maximum

$$v_{OUT\max}\left(1\right) = \frac{C_1}{C_1 + C_2} V_m \sin \omega \tau_1 - \frac{I_{OUT}}{C_1 + C_2} \left(\tau_1 - \frac{\varphi_0}{\omega}\right)$$

$$\approx \frac{C_1}{C_2} V_m \sin \omega \tau_1 - \frac{I_{OUT}}{\omega C_2} \left(\frac{\pi}{2} - \varphi_0\right).$$
(19)

Application of (19) to (15) estimates the number of periods *T* necessary for the circuit to enter steady-state:

$$k \leq 1 + \frac{C_2 V_Z - C_1 V_m + \frac{I_{OUT}}{\omega} \left(\frac{\pi}{2} - \varphi_0\right)}{2 \left(C_1 V_m - \pi \frac{I_{OUT}}{\omega}\right)}.$$
 (20)

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B. Input voltage phase is $\omega \tau_1 \leq \varphi_0 \leq \pi$

Since the input voltage at the circuit's turn-on is positive, there is an irregular commutation at the capacitors C_1 and C_2 through diode D1, so the output voltage leaps to the first local maximum

$$V_{OUT \max}(1) = \frac{C_1}{C_1 + C_2} V_m \sin \varphi_0.$$

Diodes D1 and D2 are turned off after the circuit turn-on, so the output voltage decreases. The diode D2 turns on when the input voltage phase is π and turns off again when the input voltage phase is $3\pi/2$. Afterwards, the diode D1 turns on and turns off again at the time instant of the second local maximum. If the output voltage is $v_{out} > 0$ before diode D1 turns on, the local maximum is

$$v_{OUT \max} (2) = \frac{C_1 C_2}{(C_1 + C_2)^2} V_m \sin \varphi_0 + \frac{C_1}{C_1 + C_2} V_m (\sin \omega \tau_1 + 1) - \frac{I_{OUT}}{C_2} \left(\tau_1 + \frac{2\pi}{\omega} - \frac{\varphi_0}{\omega} \right) \approx \frac{C_1}{C_2} V_m (2 + \sin \varphi_0) - \frac{I_{OUT}}{\omega C_2} \left(\frac{5\pi}{2} - \varphi_0 \right).$$
(21)

If the output voltage falls to zero before diode D1 turns on, the local maximum is

$$v_{OUT \max}(2) = \frac{C_1}{C_1 + C_2} V_m \left(\sin \omega \tau_1 + 1\right) - \frac{I_{OUT}}{C_1 + C_2} \left(\tau_1 + \frac{5\pi}{2\omega}\right)$$
$$\approx 2 \frac{C_1}{C_2} V_m - \frac{I_{OUT}}{C_2} \pi.$$
(22)

The boundary initial phase distinguishing the two variants can be determined from the equation

$$v_{OUT \max}(1) - \frac{I_{OUT}}{C_2} t_B = 0, \quad t_B = \frac{1}{\omega} \left(\frac{3\pi}{2} - \varphi_B\right),$$

that is

$$\frac{C_1 C_2}{C_1 + C_2} \frac{\omega V_m}{I_{OUT}} \sin \varphi_B = \frac{3\pi}{2} - \varphi_B.$$
 (23)

If solution of (23) is $\varphi_B < \pi/2$, then we formally set $\varphi_B = \pi/2$ and if $\varphi_B > \pi$ we formally set $\varphi_B = \pi$.

Application of (21) to (17) yields

$$k \leq 2 + \frac{C_2 V_Z - C_1 V_m \left(2 + \sin \varphi_0\right) + \frac{I_{OUT}}{\omega} \left(\frac{5\pi}{2} - \varphi_0\right)}{2 \left(C_1 V_m - \pi \frac{I_{OUT}}{\omega}\right)}, \frac{\pi}{2} < \varphi_0 < \varphi_B$$

$$(24)$$

and application of (22) to (17) yields to

$$k \leq 2 + \frac{C_2 V_Z - 2C_1 V_m + \pi \frac{I_{OUT}}{\omega}}{2\left(C_1 V_m - \pi \frac{I_{OUT}}{\omega}\right)}, \varphi_B < \varphi_0 < \pi .$$
(25)

C. Input voltage phase is $\pi \le \varphi_0 \le 3\pi/2$

Since the input voltage at turn-on is negative, there is an irregular commutation at the capacitor C_1 through diode D2, but the output voltage does not change. The series diode D1 turns on when the input voltage phase is $3\pi/2$, and the output voltage increases until the local maximum in the second cycle of the input voltage is reached, already given with (22). The start-up time is given by (25) for every φ_0 in the range.

D. Input voltage phase is $3\pi/2 \le \varphi_0 \le 2\pi$

The input voltage at turn-on is negative, and there is an irregular commutation at the capacitor C_1 through diode D2. Next, since the input voltage increases, diode D1 turns on and the output voltage starts to increase until it reaches the local maximum in the second cycle of the input voltage

$$\psi_{OUT\,\max}\left(2\right) = \frac{C_1}{C_1 + C_2} V_m\left(\sin\omega\tau_1 - \sin\varphi_0\right) - \frac{I_{OUT}}{C_1 + C_2} \left(\tau_1 + \frac{2\pi}{\omega} - \frac{\varphi_0}{\omega}\right)$$
$$\approx \frac{C_1}{C_2} V_m\left(1 - \sin\varphi_0\right) - \frac{I_{OUT}}{\omega C_2} \left(\frac{5\pi}{2} - \varphi_0\right).$$
(26)

Application of (26) to (17) yields

$$k \le 2 + \frac{C_2 V_Z - C_1 V_m \left(1 - \sin \varphi_0\right) + \frac{I_{OUT}}{\omega} \left(\frac{5\pi}{2} - \varphi_0\right)}{2 \left(C_1 V_m - \pi \frac{I_{OUT}}{\omega}\right)}.$$
 (27)

The actual k in (20), (24), (25), and (27) is an integer number, therefore we need to round up the obtained k.

III. WORST CASE START-UP TIME OF HWCDPS

The total time passed from the circuit turn-on until the moment Zener diode DZ breaks down for the first time, consists of one incomplete first cycle, $\lceil k-2 \rceil$ full cycles, and a residual of aforementioned uncertainty of the actual position of the breakage moment around the start of the k^{th} cycle of the input voltage

$$T_{S} = \frac{2\pi - \varphi_{0}}{\omega} + \left\lceil k - 2 \right\rceil \frac{2\pi}{\omega} + \varepsilon = \left\lceil k - 1 \right\rceil \frac{2\pi}{\omega} - \frac{\varphi_{0}}{\omega} + \varepsilon, (28)$$

where $\varepsilon \in \left[-\pi/2\omega, \pi/2\omega \right].$

On the basis of the feature of *ceil* function $x \le \lceil x \rceil < x+1$ and range of uncertainty ε , the start-up time can be bounded

$$(k-1)\frac{2\pi}{\omega} - \frac{\varphi_0}{\omega} - \frac{\pi}{2\omega} = T_{SLB} < T_S < T_{SHB} = k\frac{2\pi}{\omega} - \frac{\varphi_0}{\omega} + \frac{\pi}{2\omega}.$$
(29)

The important feature of HWCDPS is the maximum of the higher boundary of its start-up time, T_{SHB} , dependent on φ_0 .

After substitution of (20), (24), (25), and (27) in (29) and its differentiation, there is

$$\frac{dT_{SHB}}{d\varphi_{0}} = \begin{cases}
-\frac{1}{\omega} \frac{C_{1}V_{m} / \pi}{C_{1}V_{m} / \pi - I_{OUT} / \omega}, & 0 \le \varphi_{0} \le \frac{\pi}{2} \\
-\frac{1}{\omega} \frac{C_{1}V_{m} (1 / \pi + \cos \varphi_{0})}{C_{1}V_{m} / \pi - I_{OUT} / \omega}, & \frac{\pi}{2} < \varphi_{0} \le \varphi_{B} \\
-\frac{1}{\omega} \frac{C_{1}V_{m} (1 / \pi - \cos \varphi_{0})}{C_{1}V_{m} / \pi - I_{OUT} / \omega}, & \frac{3\pi}{2} < \varphi_{0} \le \frac{3\pi}{2} \\
-\frac{1}{\omega} \frac{C_{1}V_{m} (1 / \pi - \cos \varphi_{0})}{C_{1}V_{m} / \pi - I_{OUT} / \omega}, & \frac{3\pi}{2} < \varphi_{0} < 2\pi
\end{cases}$$
(30)

In the range of the initial phase $0 \le \varphi_0 \le \pi/2$, T_{SHB} monotonically decreases with the maximum value for $\varphi_0 = 0$

$$T_{SHB}(0) = \frac{\pi}{2\omega} \frac{2C_2 V_Z + 3C_1 V_m - 4\pi \frac{I_{OUT}}{\omega}}{C_1 V_m - \pi \frac{I_{OUT}}{\omega}}.$$
 (31)

In the range of the initial phase $\pi/2 < \varphi_0 \le \varphi_B$, T_{SHB} has a local minimum at $\varphi_{\min 1} = \arccos(-1/\pi) \approx 1.25$ rad, if $\varphi_B \ge \varphi_{\min 1}$.

$$T_{SHB}\left(\varphi_{1\min}\right) = \frac{\pi}{2\omega} \frac{2C_2 V_Z + C_1 V_m \left(5 - 2\frac{\varphi_{1\min}}{\pi} - 2\sin\varphi_{1\min}\right) - 4\pi \frac{I_{OUT}}{\omega}}{C_1 V_m - \pi \frac{I_{OUT}}{\omega}}$$

In the third case, when the initial phase is in the range $\varphi_B < \varphi_0 \le 3\pi/2$, T_{SHB} again monotonically decreases, with maximum value for $\varphi_0 = \varphi_B$

$$T_{SHB}\left(\varphi_{B}\right) = \frac{\pi}{2\omega} \frac{2C_{2}V_{Z} + C_{1}V_{m}\left(5 - 2\frac{\varphi_{B}}{\pi}\right) - \frac{I_{OUT}}{\omega}(7\pi - 2\varphi_{B})}{C_{1}V_{m} - \pi \frac{I_{OUT}}{\omega}}.$$
(32)

It is impossible to solve (32) manually, since φ_B is given by transcendent equation (23), but it may be enough to compare maximum possible value of (32), for minimum $\varphi_B = \pi/2$, and (31). Therefore, maximum (32) is

$$T_{SHB}\left(\varphi_{B}=\frac{\pi}{2}\right)=\frac{\pi}{2\omega}\frac{2C_{2}V_{Z}+4C_{1}V_{m}-6\pi\frac{I_{OUT}}{\omega}}{C_{1}V_{m}-\pi\frac{I_{OUT}}{\omega}}.$$
 (33)

From (23) there is the relation valid for $\varphi_B = \pi/2$, $I_{OUT} = \frac{C_1 C_2}{C_1 + C_2} \frac{\omega V_m}{\pi} \approx C_1 \frac{\omega V_m}{\pi}$, that is readily substituted in nominators of both (32) and (33), so the two are easy to compare

$$T_{SHB}(0) \left| \varphi_B = \frac{\pi}{2} = \frac{\pi}{2\omega} \frac{2C_2 V_Z - C_1 V_m}{C_1 V_m - \pi \frac{I_{OUT}}{\omega}} \right|$$

$$> \frac{\pi}{2\omega} \frac{2C_2 V_Z - 2C_1 V_m}{C_1 V_m - \pi \frac{I_{OUT}}{\omega}} = T_{SHB} \left(\varphi_B = \frac{\pi}{2} \right)$$
(34)

Within the range $3\pi/2 < \varphi_0 \le 2\pi$, T_{SHB} has a local minimum at $\varphi_{\min 2} = \arccos(1/\pi) = \varphi_{\min 1} + \pi = 4.39$ rad. The T_{SHB} value at this local minimum equals the T_{SHB} value at the local minimum $\varphi_{\min 1}$, $T_{SHB}(\varphi_{\min 2}) = T_{SHB}(\varphi_{\min 1})$. The T_{SHB}

value at the right boundary of the range, when $\varphi_0 \rightarrow 2\pi$, equals the T_{SHB} maximum value at $\varphi_0 = 0$. The T_{SHB} value at the left boundary of the range, when $\varphi_0 = 3\pi/2$, is less than (33), that is less than (31) as shown in (34).

As an illustration, the dependency $T_{SHB}(\varphi_0)$ is plotted in Fig. 5 for $C_1 = 420$ nF, $C_2 = 22 \mu$ F, $V_m = 300$ V, $\omega = 314$ rad/s, $V_Z = 15$ V and $I_{OUT} = 10$ mA. The characteristic value of initial phase is $\varphi_B \approx 2.57$ rad.

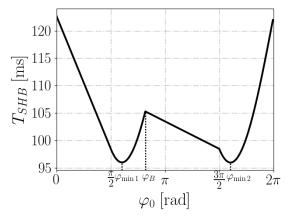


Fig. 5. Typical dependence of higher bound of start-up time T_{SHB} on initial phase φ_{0} .

On the basis of the previous analysis, the worst case estimation of start-up time of HWCDPS, over entire range of initial phase φ_0 and uncertainty of the actual position of the Zener diode breakage moment is

$$T_{S} \leq \frac{\pi}{2\omega} \frac{2C_{2}V_{Z} + 3C_{1}V_{m} - 4\pi \frac{I_{OUT}}{\omega}}{C_{1}V_{m} - \pi \frac{I_{OUT}}{\omega}}.$$
 (35)

IV. SIMULATION

A series of LT SPICE simulations for various values of V_Z , C_1 , C_2 , I_{OUT} , and φ_0 were conducted. We used the diode 1N4148 for the diodes D1 and D2, and members of BZX84C Zener diode family for DZ. Input voltage features were $V_m = 300$ V and $\omega = 314$ rad/s.

In order to make a consistent comparison, because of the Zener diode voltage resistance, we defined actual start-up time as the time interval passed from the circuit turn-on until the output voltage reaches the Zener diode nominal breakdown voltage for the first time.

We compared the estimated worst case start-up time (35), and the actual start-up time over the series of simulations. In every simulation, the difference between the two is less than one cycle of the input voltage T = 20 ms, as illustrated in the Table I for $V_Z = 15$ V. Given the inevitable uncertainty of the actual position of the Zener diode breakage moment is one half of the input voltage cycle, this represents a very good estimation. The missing data in the Table I is due to the limitation (18), meaning that, for some given I_{OUT} and V_Z , there is a minimum value of C_1 for Zener diode in a HWCDPS to start to break down periodically. For $I_{OUT} = 10$ mA and $V_Z = 15$ V, (18) gives $C_1 \ge 342$ nF.

TABLE I COMPARISON OF ESTIMATED WORST CASE START-UP TIME AND THE START-UP TIME OBTAINED FROM SIMULATIONS, FOR V_Z = 15 V

C_1	C_2	IOUT	<i>T_{SHB}</i> [ms] (35)	T_s [ms] (SPICE)	ΔT_s [ms]
330 nF	10 µF	2 mA	32.7	20	12.72
		5 mA	40.5	22.7	17.8
		10 mA	-	-	-
	22 µF	2 mA	55.5	40.9	14.6
		5 mA	77.2	62.1	15.1
		10 mA	-	-	-
	47 µF	2 mA	103	97.7	5.3
		5 mA	153.8	141.8	12
		10 mA	-	-	-
470 nF	10 µF	2 mA	26.6	18	8.6
		5 mA	28.7	19.5	9.2
		10 mA	39.4	22.1	17.3
	22 µF	2 mA	41.4	22.6	18.8
		5 mA	48.5	39.6	8.9
		10 mA	83.3	80.7	2.6
	47 µF	2 mA	72.4	60	12.4
		5 mA	89.7	80	9.7
		10 mA	174.8	163.4	11.4
680 nF	10 µF	2 mA	22.6	3	19.6
		5 mA	23.1	3.4	19.7
		10 mA	24.6	19.3	5.3
	22 µF	2 mA	32.4	19.7	12.7
		5 mA	34.8	20.7	14.1
		10 mA	41.9	23.1	18.8
	47 μF	2 mA	52.8	39.9	12.9
		5 mA	59.2	42	17.2
		10 mA	78	62.6	15.8

V. CONCLUSION

The developed formula (35) for the worst-case start-up time of HWCDPS shows a good correlation with simulation results, since the difference between estimated and simulated start-up time is less than one cycle of the input voltage. Given tolerances of the rated capacitance values, (35) provides for a sufficiently accurate characterization of HWCDPS in sense of the circuit's inertia after turn-on.

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REFERENCES

- N. Mohan, T. M. Undeland, and E. P. Robbins, *Power Electronics: Converters, Applications and Design*, 2nd edition, New York, NY: John Wiley & Sons, 1995.
- [2] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd edition, Secaucus, NJ: Kluwer Academic Publishers, 2000.
- [3] S. D'Souza, 'Transformerless Power Supply', Microchip Technology Inc., Chandler, AZ, App. Note TB008, 2000.
- [4] R. Condit, 'Transformerless Power Supplies: Resistive and Capacitive', Microchip Technology Inc., Chandler, AZ, App. Note AN954, 2004.
- [5] 'Low-cost Power Supply for Home Appliances', STMicroelectronics, Geneva, Switzerland, App. Note AN1476, 2004.
- [6] V. M. Rajović and N. S. Jovičić, "The capacitive divider power supply and its design problem," in *Proc. Telecommunications Forum* (*TELFOR*), 2011, pp. 852–855.