On the implementation of modern power transistors in low-voltage circuit breakers

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***Abstract*—Conventional circuit breakers suffer from two main deficiencies: they are slow to operate and develop an electrical arc. These may be overcome by using solid-state switches which in turn introduce other problems, most significantly power dissipated while in the on-state. Nevertheless, a number of solid state devices are candidates for implementation as low-voltage circuit breakers and there are several options based on the semiconductor material that may function as high-power switches. We present a unique, extensive and systematic evaluation of these options for suitability as solid state breakers. Voltage controlled devices are selected due to the simplicity of the controlling circuit and their resilience to d*v*/d*t* induced switching. Properties of fully solid-state circuit breakers are established and systematic comparisons are made among switches built of silicon and several other wide band-gap (WBG) devices such as SiC MOS and GaN HEMT transistors. Using SPICE simulation of transistor models supplied by the device manufacturers, it is shown that solid state circuit breakers (SSCBs) based on WBG devices exhibit superior characteristics compared with silicon devices, with faster switching and higher voltage and current ratings.**

***Index Terms*—Solid-state, wide band gap semiconductor, power transistor, circuit-breaker, switch, power systems, low-voltage grid, cable.**

I. Introduction

Worldwide, low-voltage power distribution networks are facing a multitude of challenges to maintain availability and quality [1]. These mainly stem from increasing distributed renewable generation connected to sustainably meet inexorable load growth. Another exacerbating factor is long term urbanisation due to migration from rural areas, leading to dense urban networks with aging assets, resulting in reliability and maintenance problems. In addition more and more stringent regulations are required based on key performance indicators such as Customer Interruptions (CIs) and Customer Minutes Lost (CMLs) [2].

Protection of the system against fault current is usually achieved by circuit breakers (CBs) [3]. If a fault condition is detected these devices de-energize the circuit protecting equipment against damaging short-circuit current. Conventional CBs (e.g. [4]) in the network protect against faults by dissipating the circuit inductive energy in the form of an arc. The arcing in conventional circuit breakers during fault clearing is essential to follow the conservation of energy law [3]. Due to arcing, however, these devices require regular maintenance and must be over-rated due to the moving mechanical parts having large time constants.

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To mitigate the consequences of an arc and improve protection response times, solid-state and hybrid circuit breakers (HCBs) have been introduced in high and medium-voltage distribution systems. The first generation of devices were thyristor based [3,5] but more recently IGBTs [6-7] were implemented for AC applications. There have also been major advances in low [8] and high-voltage DC solutions [9].

Recently, as an alternative to the thyristor and its derivatives, wide band-gap (WBG) semiconductors have been used for power conversion, particularly electrical vehicles and in renewable generation [10]. While some solutions of SSCBs for DC power systems exist [8,11], implementation of WBG semiconductors in low-voltage AC CBs, to the best knowledge of the authors, have not yet been reported in the literature.

The goal of this research was to investigate the circuit solutions using modern WBG devices for low-voltage circuit breakers, and to compare standalone systems (as SSCBs) with HCBs built with a combination of conventional and solid-state technology. To that end, the most important task was to establish the properties and the behavior of a power switch built from WBG semiconductors.

The paper is structured as follows. Firstly voltage controlled and current controlled devices are compared for suitability for implementation in SSCBs. After a short overview of the properties of WBG semiconductors, the behavior of the switches constructed of voltage controlled transistors are studied. Then SSCBs and HCBs, built with four commercially available devices are simulated using SPICE and compared. It is shown that SSCB may act very quickly and may be successfully used for very fast protection. The price paid is the power consumed while the switch is in on state which, for the example system discussed here, was found to be not lower than 0.5% of the source power.

II. Choice of switching device

There are two categories of electronic devices which may be used as a switch: current-controlled (CC) and voltage-controlled (VC). Thyristors need a current pulse at the gate terminal to enable switching-on. Ordinary for thyristors, GTOs and IGCTs relatively complex control circuits are required to facilitate the CB's operation. (Similar stands for the SiC JFET as stated in [11].) In addition fast change of the anode voltage (dv_A/dt) of a thyristor can provoke switching-on as is illustrated in Fig. 1a. Here, when in off-state, a capacitive current (proportional to the derivative of the voltage) is established (denoted i_{p3}) which charges the depletion capacitance C_{GK} of the gate-to-cathode p-n junction. It may provoke

conduction of the p-n junction and, consequently, firing the thyristor at relatively *low anode voltages* while the gate terminal is disconnected.

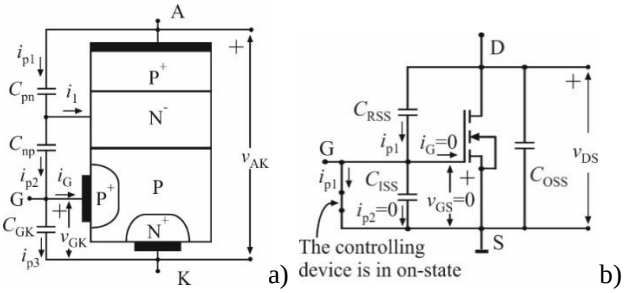

Fig. 1. (d*v*/d*t*) firing of a thyristor (a) and reluctance of a voltage controlled device (b)

That is not the case when VC devices are used, for example the N-channel enhancement mode metal-oxide-semiconductor field-effect-transistor (Si MOS) depicted in Fig. 1b. Here, to keep the transistor in the off-state the input terminals (gate and source) are short-circuited by a controlling device so that no charging of C_{ISS} occurs.

For these reasons only VC devices are considered further: the Si MOS, the gallium-nitride high electron mobility transistor (GaN HEMT), the silicon carbide MOS (SiC MOS) and the silicon insulated gate bipolar transistor (Si IGBT). For simulation purposes the models of the Si MOS R5021ANX [12], the Si IGBT NGTB30N135IHRWG [13], the SiC MOS C3M0065090D [14], the GaN HEMT EPC2027 [15], and the GaN HEMT GS66516T [16] were used. For all of these SPICE [17] models are publicized by the producers.

III. WIDE BAND-GAP SEMICONDUCTORS

Solid-state devices are based on semiconductor materials which evolved over time through several phases [18]. Germanium (Ge) was the so-called first generation material while silicon (Si) was the second. The third generation of semiconductors, consisting of materials such as 4H-SiC and GaN, is currently under development and will yield new devices with improved capabilities related to frequency, current, voltage, power, and working temperature ratings

TABLE I. BASIC PHYSICAL AND ELECTRICAL PROPERTIES OF SELECTED SEMICONDUCTOR MATERIALS

Material	$E_{g\ \|T=300K}$ (eV)	$n_{i\ \|T=300\ K}$ (10^{10}. cm^{-3})	T_{max} (°C)	Θ $\left(\frac{W}{cm\cdot K}\right)$	v_{sat} (m/s)
Si	1.12	1.45	200	1.5	$1\cdot10^7$
4H-SiC	3.26	10^{-4}	600	4.9	$2\cdot10^7$
GaN	3.5	10^{-10}	400 -900	1.3	$2.5\cdot10^7$

Material	K_s $\left(\frac{MV}{m}\right)$	K_c $\left(\frac{MV}{m}\right)$	μ_n $\left(\frac{cm^2}{V\cdot s}\right)$	ρ (intr.) (MΩ·cm)	ρ* (n-type) (Ω·cm)
Si	6	300	1450	0.23	0.53
4H-SiC	10	3,500	900	1000	1
GaN	20	3,300	2000**	Inf.	0.01

*ρ (n-type) was measured for: $N_D=10^{16}$ cm^{-3} in Si; $N_D=10^{18}$ cm^{-3} in 4H-SiC; and $N_D=10^{19}$ cm^{-3} in GaN. ** μ_n stands for the 2DEG.

From an electrical conduction point of view the most important physical parameter of a material is its band-gap (E_g). It defines the concentration of free charge carriers in an intrinsic material (n_i) and so its electrical conductivity. Table 1. depicts the values of E_g and n_i for the three semiconductors. As can be seen 4H-SiC and GaN have about a three-fold wider band-gap than Si.

The difference in the value of n_i may also be recognized from the value of the resistivity (ρ) of intrinsic semiconductors. It also defines the maximal temperature, T_{max}. By adding impurities the resistivity of a semiconductor is dramatically changed. The values of ρ were taken from the literature such as [19]. These are also related to the mobility of the majority carriers (μ_n). This resistivity value, however, at high fields (above the saturation electrical field K_s), is increased due to the limitation of the carrier velocity (v_{sat}). Finally, the maximum voltage on a pure semiconductor is defined by the critical field K_c while the thermal conductivity (Θ) expresses the delivery of the dissipated heat to the surroundings of a thermal source located within the material. Looking to the numerical values, there are obvious differences between the materials of the second and third generation which makes the latter more convenient for high power, high voltage, and high current applications.

Different technologies, however, are required to produce the semiconductors of the second and third generation [20]. These considerations bring to the fore issues surrounding price and reliability and thus at present limit the widespread implementation of WBG materials.

The most common sub-structure of a solid-state device is the p-n junction. For power and switching applications its most important property is the breakdown voltage. It may be approximately expressed as: $V_B=(\varepsilon\cdot K_c)/(2\cdot q\cdot N)$, where N is the majority concentration at the lightly doped side, ε is the dielectric constant of the semiconductor and q is the charge of the electron. This expression takes the form $V_B=\alpha\cdot10^{17}/N$, where α= 2.96 for Si; α= 135 for 4H-SIC; and α= 99.4 for GaN diode [21]. Obviously, significant rise of the breakdown voltage of a p-n junction may be obtained by using WBG semiconductors.

III. VOLTAGE CONTROLLED TRANSISTORS AS POWER SWITCHES

Fig. 2 represents a cross section of one example, N-channel the enhancement mode Si MOS transistor. This structure is used to analyze suitability of the Si MOS in high power applications.

High voltage devices are obtained by the insertion of the N^- region (low concentration). This in it turn raises the resistance of the body of the drain thus increasing the on-resistance of the device. Accordingly, the breakdown voltage and the on-resistance are highly correlated quantities. High currents are achieved by parallel connection of many Si MOS transistor on a silicon chip.

The structure of the SiC MOS transistor is fundamentally

the same.

The GaN HEMT may be more properly characterized as MES (metal-semiconductor) FET. Namely, instead of the insulator (oxide), between the substrate (GaN) and the metal gate, a layer of GaAlN is inserted which forms a heterojunction with the GaN substrate. Just below the GaAlN layer the so-called 2DEG (two dimensional electron gas) is formed as a consequence of the nature of the heterojunction. It serves as the channel of the device. The main property of the 2DEG is its high mobility which allows for production of both fast and high current devices.

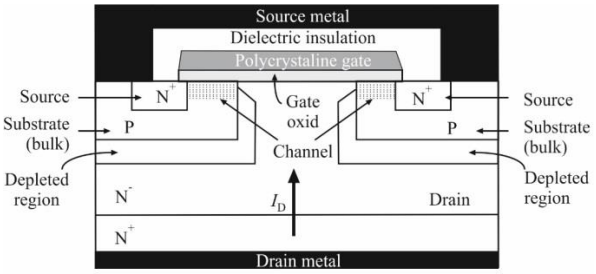

Fig. 2. Cross section of an enhancement type N-channel VDMOS

Finally, the IGBT (insulated gate bipolar transistor) is a silicon device with a specific connection of a MOS and a BJT (bipolar junction transistor).

For the switching speed and perspective of transient behavior, the most important characteristics of the transistors are their capacitances.

TABLE II. POWER TRANSISTOR CAPACITANCES (IN PF)

Type	C_{ISS}	C_{RSS}	C_{OSS}
SiC MOS (V_{DS}=600 V) C3M0065090D	660	4	60
GaN HEMT (V_{DS}=360 V) EPC2027	180	0.02	23
Si MOS (V_{DS}=25 V) R5021ANX	2300	70	1000
Si IGBT (V_{AK}=20 V) NGTB30N135IHRWG	5290	100	124

With reference to Fig. 1b, in device datasheets, the following capacitances may be found: the input capacitance C_{ISS}, the reverse transfer capacitance (or Miller capacitance) C_{RSS}, and output capacitance C_{OSS}. Table 2. depicts measured values of the transistor capacitances for Si, GaN, and SiC based power transistors (partly taken from [22] and partly from original datasheets). The measurements are performed for different working conditions, the values from this table should be taken for qualitative comparison only. As can be seen the values differ in favor to GaN and SiC.

Among the capacitances discussed, C_{ISS} is of special importance since it contains the Miller capacitance between the output and the input terminal (C_{GD} for the unipolar devices). Namely, the current of the Miller capacitance of the circuit of Fig. 3 (assuming C_{GD} is voltage independent) can be calculated using

$$i_C = C_{GD} \cdot \frac{d}{dt}(v_G - v_D) = C_{GD} \cdot (1-G) \cdot \frac{dv_G}{dt} \quad (1)$$

where v_D and v_G are node voltages of the drain and the gate terminal, respectively, and G is the incremental gain which is here negative. From this expression two important conclusions may be drawn. First, G is strongly dependent on the input voltage. Following the load line, it starts with G=0 for $v_G<V_T$, goes through its maximal value for values of v_G and v_D belonging near the upper edge of the active region, and falls again to zero in the ohmic region. This is depicted in Fig. 4 (bottom line) for the circuit of Fig. 3 with no reactive elements included i.e. for k small number and L=0 H. Consequently, both the equivalent capacitance C_{GD}·(1-G) and the input capacitance C_{ISS} are strongly nonlinear.

Second, Fig. 4 (top line) depicts the power dissipation at the transistor during switching. It may be observed that while the transistor's working point traverses the active region the dissipated power reaches high values. Care should be taken not to exceed the rated pulsed maximal power of the transistor. Namely, none of the above mentioned transistors may sustain 2 kW continuously which may be seen from the safe operation area (SOA) given in the datasheets of each. When fast switching happens, larger powers are allowed. For example, for the GS66516T to sustain 2 kW the transition should be as short as 100 μs. For the same duration of the pulse the maximum power allowed for the Si MOS R5021ANX is 1.2 kW.

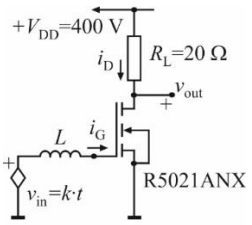

Fig. 3. The test circuit for switching-on the transistor

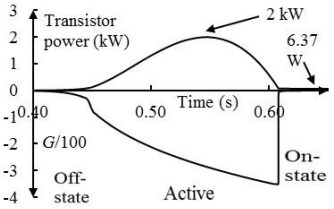

Fig. 4. The test circuit, (bottom) static (no reactive circuit and model elements included) incremental gain (G) of the inverter and (top) power consumption of the transistor

When switched-on the transistor is consuming some power, albeit small. This is the minimum power which it would consume if used in a circuit breaker (for the Si MOS R5021ANX it is 6.37 W). The power loss is related to the value of the transistors on-resistance denoted as r_{DSon} which becomes an important parameter of a transistor. Its value is dependent on the I_D (as is the minimum voltage) which, for the circuit of Fig. 3, is 20 A. The larger the current, the larger r_{DSon}.

Looking to the transients, the value of the input current is strongly dependent on the slope of the input signal or, in other words, on the speed of switching. To illustrate, in Fig. 5a and Fig. 5b the (overall) input current of the circuit of Fig. 3 (for the Si MOS R5021ANX) as a function of time is depicted for k=100 V/ms and k=500 V/ms, respectively. Significant rise of the peak value of the input current may be observed. Also from the Fig. 5, one may conclude that larger values of

parasitic inductances may lead to oscillating switching.

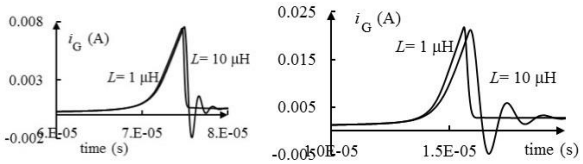

Fig. 5. Influence of the input capacitance and a parasitic inductance to the input current of an inverter. Left: k=100 V/ms and right k=500 V/ms

In a solid state circuit breaker switching-off the electronic device is of major concern. To get a basic notion of the problem, here the circuit of Fig. 6 was simulated. It is the same as that depicted in Fig. 3 except that the input voltage source is substituted by a driving circuit modelling the output of an opto-coupler. The open switch in the gate circuit of Fig. 6 means that the transistor is in the on-state. When the switch is closed the gate voltage becomes reduced to the on-voltage of the diode (below the transistor's threshold voltage) which leads the transistor in cut-off.

The simulation results (for the Si MOS R5021ANX) for L=5 µH are depicted in Fig. 7a. The switch was turned on at t=10 µs with its own transition time of 1 ps. Delay time of approximately 270 ns along with a rise time (or transition time) of approximately 80 ns may be observed. In order to check the origin of the shape of the waveform an additional simulation was conducted with the diode short circuited. No noticeable changes were found confirming that it is the transistor alone that fully defines the switching.

Fig. 7b depicts the same time domain response but with L=15 µH. Due to the transient in the gate circuit a negative pulse is added to the output voltage. This is more pronounced when L is raised such that additional pulses are observed due to oscillations in the gate circuit.

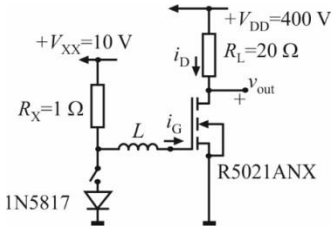

Fig. 6. Test circuit for switching-off

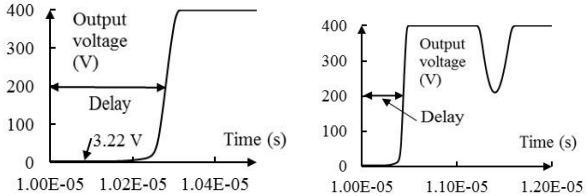

Fig. 7. Left: Output voltage (L= 5 µH), and Right: Output voltage (L= 15 µH)

Finally, from Fig. 7a one may find out the minimum value of the drain-to-source voltage of the transistor being approximately 3.22 V (under the condition of R_L=20 Ω and V_{DD}=400 V). This is important since it represents the voltage drop on the closed switch.

Simulations of the circuit of Fig. 6 were performed for all four transistors mentioned above. The results are summarized in Table 3. Here some circuit parameters are given (V_{xx} and the maximum value of L that is able to avoid oscillations during switching) together with electrical and timing data.

TABLE III. SWITCHING OFF A POWER TRANSISTOR

Type of transistor	V_{xx} (V)	Max. L (µH)	Voltage in on-state (V)	Delay time (ns)	Rise time (ns)
SiC MOS C3M0065090D	20	1	1.15	25	10
GaN HEMT EPC2027	5	0.001	8.42	0.92	1
Si MOS R5021ANX	10	15	3.22	270	80
Si IGBT NGTB30N135IHRWG	15	0.5	2	320	600

Note that the switching times are in the nanosecond region i.e. incomparably faster than any mechanical switch. While the HEMT allows for fastest switching the SiC MOS exhibits the smallest on-voltage which is of importance for switches being normally in the on-state.

It may be seen from Table 3. that a HEMT based switch is extremely sensitive to the lead inductances. This issue is incomparably less influential if Si MOS transistors are considered. However, final conclusions cannot be drawn based solely on the numbers depicted in Table 3. Namely, the importance of the information depicted will depend on how the transistor is implemented in a CB. As will be shown later on, different parameters play the main roles in SSCBs and in HCBs.

IV. SOLID STATE CIRCUIT BREAKERS

A simplified schematic of a SSCB is depicted in Fig. 8 It is based on the one proposed in [23] and is also reminiscent of that described in [6]. Note, the schematic symbols for the switches (denoted by S1 and S2) serve here only as substitution for the real switches constructed by proper arrangement of transistors and other circuit elements [24]. In fact the switch is built of two transistors with their sources and gates connected together while the switch terminals are the drains of the two. The voltage ratings of such a switch are twice as high as the voltage ratings of a single transistor and for low-voltage applications (<1 kV) all technologies (silicon and WBG) are satisfactory. A controlling circuit (the branch V_{XX}-R_X-photosensitive switch), depicted in Fig. 6, is added to complete the switch.

The functionality of this circuit may be described as follows [23]. "At start-up, S1 opens first and once steady state is reached, S2 is switched on. Because of the higher resistance R, the current will flow through S2 instead of S1. With this design high start-up currents are limited. S1 is kept on but due to the resistance R only a negligible part of the current will flow through it. If an overload (the load switches from R_{L1} to R_{L2}, the latter being much smaller) or a current transient occurs, the controller creating the SS2 signal turns S2 off and R prevents overcurrent. If the fault condition lasts longer than

the programmed time-current ($(I\cdot\tau)_{max}$) curve allows, S1 will also be turned off and completely break the circuit."

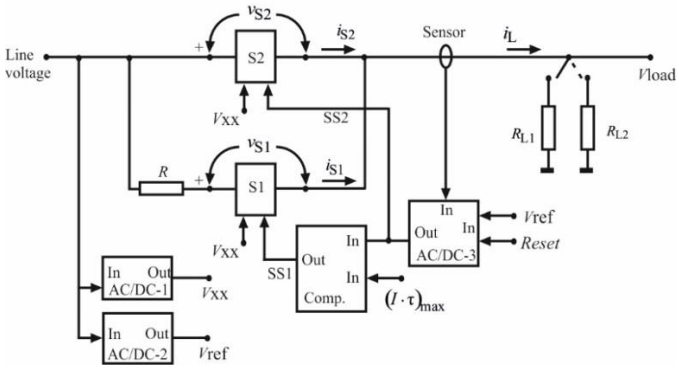

Fig. 8. Simplified schematic of the MOS transistor based circuit breaker

The AC/DC-1 and AC/DC-2 converters depicted on the left hand side produce DC voltages for a) supplying DC voltage (V_{xx}) to the input circuit of the switches and b) the reference voltage (V_{ref}) necessary for comparison in order to activate the switch S2, respectively. The AC/DC-3 circuit first converts the output current into a DC time varying voltage signal V_{int}. The circuit then compares this with V_{ref}, and finally, when V_{int} exceeds V_{ref}, it triggers the state of SS2 from 0 to 1 which will last until a *Reset* signal is presented to the input.

The Comp. circuit is activated by SS2 and compares the actual $I_{eff}\cdot t$ value (I_{eff} is the rms value of i_L) with the prescribed $(I\cdot\tau)_{max}$ value to produce the SS1 signal which completely switches off the circuit breaker.

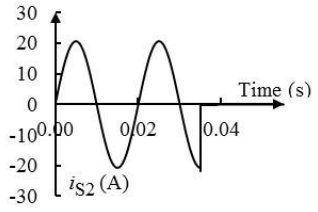

Fig. 9. Instantaneous value of I_{s2} as a function of time (SiC MOS used in the switch)

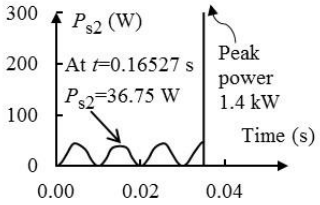

Fig. 10. Instantaneous power of S2 (SiC MOS used in the switch)

The simulation result for the instantaneous value of the current of S2 (i_{S2}), for the case when the SiC MOS (C3M0065090D) transistors were used in the switch, are depicted in Fig. 9. As can be seen, S2 is activated when the peak current of 22 A is reached.

The overall switching time (T_{offS}, from the moment when the fault occurs until i_{S2} falls to zero) and the time needed for S2 to change state are different due to the delay in the controlling loop as can be seen in Table 4. Results are obtained by simulation of circuits where S2 was the particular transistor shown. Due to the differences in the properties of the transistors V_{XX} and V_{ref} required adjusting for each case.

As expected the fastest switching of S2 (T_{offT}) was observed when GaN HEMT was implemented while the Si MOSFET was the slowest. The situation is changed when the overall delay (T_{offS}) is considered, with SiC MOSFET becoming fastest and the IGBT the slowest. One should have in mind that no other optimizations were done in the controlling circuit to accommodate the properties of the transistors except for those mentioned (V_{ref} and V_{XX}).

TABLE IV. COMPARISON OF THE MAIN PROPERTIES OF THE SOLID-STATE SWITCHES*

Component	P_{av} (W)	P_{rel} (%)	T_{offS} (ns)	T_{offT} (ns)	INF
SiC MOSFET, C3M0065090D	10	0.5	100	35	Low
GaN HEMT, EPC2027	125	6.25	155	8	Very high
Si MOSFET, R5021ANX	20	1	320	300	High
Si IGBT, NGTB30N135IHRWG	12.5	0.625	1500	200	Very high

* P_{av} [Average power per transistor when in on-state]; P_{rel} [Relative average power per switch when in on-state]; T_{offS} [Overall Switching-off (the breaker) time]; T_{offT} [Switching- off (the Transistor) time]; and INF [Influence of the (input circuit) inductances to switching-off time]

Probably the most important information given in Table 4. is P_{av}, the approximate value of the average power dissipated per transistor before switching-off. This value was obtained from the peak value (as shown in Fig. 10 for the case when SiC MOS was used in the switch) by dividing it by 4. Its importance is due to the CB being normally in the on state when the system is energized under normal operational conditions. This means that a large amount of energy is consumed while the CB is idle, giving large operational expenditure. The SiC based SSCB is preferable from this point of view.

P_{rel} in Table 4. is related to the power consumed by the switch, while it is in on-state, divided by the source power and expressed as a percentage. In the case of the SiC CMOS switch, only less than half a percent of the source power is consumed by the switch which is in agreement (while slightly smaller) with the results reported in [8], where low DC voltage bidirectional switch based on SiC JFET is described. While for low DC voltage applications this number is probably acceptable, here, for AC power electrical systems when large loads are fed, there is a necessity for parallel connection of the solid state switches. If one needs m parallel branches to build the switch, then the consumed power will be $2\cdot m\cdot P_{av}$ while the percentage (P_{rel}) will stay the same. Accordingly, even the value of 10 W per transistor may become, in general, prohibitive for most applications. Similar considerations are important when higher voltages are to be switched where series connection of switches will be necessary. In such cases, the maximum fault current can be set to be not much larger than the maximum load current in normal operation and consequently the protection may become extremely effective.

A power surge may be noticed in Fig. 10 during the period of switching. Its value is 1.4 kW (i.e. 0.7 kW per transistor) and its duration (Table 4.) is 100 ns. Since, however, the allowed pulsed power for pulses shorter of 10 μs is 6 kW [14], this will be not considered as a problem.

Finally, the influence of the input inductance in the system was investigated. First, partly inductive load was switched with no obvious effects on the switching waveforms. Much greater significance was shown to lie with the inductance in the input circuit of the switch. The qualifications in the last column of Table 4. are based on comparisons of waveforms of the voltages during switching-off similar to the one depicted in Fig. 7b (which was given for a single transistor DC switching). As may be seen from Table 4. in most of the cases, care is to be taken to eliminate its influence (for example, by reducing its value).

V. Conclusion

It was the intention of this study to make the first steps in the investigation of the applicability of WBG semiconductor devices in LV CBs. Thus four voltage controlled transistors were selected and investigated for their behavior as switches. The SSCB circuit was synthesized and analyzed for all four cases. To complete the picture, a short study of hybrid CBs was given together with corresponding simulation results. The main findings may be summarized as follows.

A mechanical or magneto-mechanical circuit breaker is characterized by three main properties. Its main advantageous property is the very low resistance when in on-state. The main action of a CB, however, is breaking or opening the circuit. For success in this operation the mechanical CB has two problems: it is relatively slow, so it may jeopardize the system which it protects, and it produces an arc which shortens its life-span and reduces reliability.

A fully solid-state circuit breaker avoids the arcing problem. It was shown in this study, however, that a very high price is paid for the elimination of the arc when a low voltage SSCB is used. Namely, the power consumed by the SSCB when in on-state is so large that it becomes prohibitive for many applications. It should be mentioned that third useful property of SSCBs is very fast switching-off. SSCBs can therefore be recommended for protection of very sensitive systems.

For conventional low voltage applications, a hybrid circuit breaker (HBC) combines the advantages of SSCBs and CBs. Here, during switching-off, in order for the parallel connection to work properly, the mechanical part is disconnected first. That means that the HCB will inevitably inherit the switching speed of the mechanical CB. Looking to the overall switching time there will be no profit for implementation of the electronic part. The SSCB part is activated (switched-off) after a delay caused by the mechanical CB and after the load current (or power) exceeds a prescribed threshold. This will allow for a parallel path that will "*extinguish*" the arc. Note, the SSCB at the beginning of its transient takes over the complete value of the short-circuit current and, at its end, the complete value of the line voltage.

According to these considerations, the SSCB part of the HCB must have all the requirements of an SSCB which would act alone except for the consumed power while in on-state since it is active very briefly.

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