# Method for measuring the settling time of integrated PLL using Spectrum Analyzer

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*Abstract*—Settling time is one of the parameters most difficult to measure, especially for integrated PLLs, since many internal, low-frequency signals are usually not available to the user. This paper describes the method for accurate measurement of settling time of integrated frequency synthesizers using the waveform capturing capabilities of modern spectrum analyzers.

*Keywords*—measurement, PLL, settling time, RFIC, spectrum analyzer

## I. INTRODUCTION

Phase Locked Loops, PLLs, are very important elements of current modern integrated radio transceivers [1]. Main purpose of PLL in these systems is to generate stable and clean carrier or clock signal, which is usually used in the modulation/demodulation processes inside the transceiver chain and/or as a clock signal in the DA/AD conversion circuits. Quality of frequency synthesizer has a very strong influence to the overall performance of complete RFIC. Generic block diagram of a typical PLL-based frequency synthesizer system is shown in Fig.1.

Today, integrated radio transceivers are often able to synthesize LO frequencies in very wide bandwidth with very fine resolution steps in order to satisfy strict requirements imposed by various standards for wireless communication. Central part of each PLL is Voltage Controlled Oscillator, VCO. VCO is an oscillator circuit whose oscillation frequency can be tuned in some range using the control voltage input. PLL is a system with negative feedback. Phase and frequency difference between signals at the output of VCO feedback frequency divider and reference signal are detected in the Phase Frequency Detector, PFD circuit. The error signal is generated based on this difference and converted to voltage using Charge Pump, CP and low-pass loop filter, LPF circuits. This voltage is connected to the VCO control input. PLL tunes the VCO frequency in order to minimize the phase/frequency difference at the PFD input [2]. In the steady state, VCO is phase locked to the very stable input reference signal, which most often comes from the external oscillator that uses quartz crystal as a resonator (XO, TCXO, VCTCXO, OCXO). Typical oscillation frequency values of crystal oscillators are in the order of tens of MHz.

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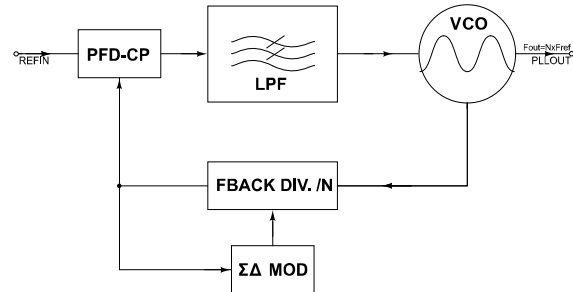Lazar Saranovac – School of Electrical Engineering, Bulevar Kralja Aleksandra 73, Belgrade, laza@el.etf.rs

Fig. 1. Block Diagram of Typical PLL-Base Frequency Synthesizer

Most commonly used measures to quantify the performance of a PLL-based frequency synthesizer are phase-noise, spur suppression and frequency settling/lock time [2]. PLL design usually involves finding the optimal trade-off between these quantities. Therefore, precise measurements of performance parameters of integrated PLL are of crucial importance to the designer as that enables him to make the final tweaking of RFIC settings in order to get the best out of transceiver.

The PLL lock time is the time that it takes the PLL to switch from one carrier frequency to another and reach the steady state. Steady state means that PLL output frequency reached the desired value within some frequency tolerance usually expressed in parts per million (ppm) of targeted value. Modern digital communication systems use frequency hopping techniques to overcome fading and increase the channel capacity. On the other hand, this technique imposes high demands on the PLL frequency settling time. During the time that PLL takes to change its output frequency, radio transceiver cannot transmit nor receive the data. So if settling time takes too long, the data rate of the system can be seriously reduced.

This paper describes one simple method to precisely measure the PLL frequency settling time using the spectrum analyzer. In chapter II, the most common methods for measuring the PLL settling time together with their main advantages and disadvantages are briefly described. Proposed measurement method is explained in more details in chapter III. Measurement results are presented in chapter IV. The conclusions are given in chapter V.

## II. USUAL METHODS FOR MEASURING THE PLL SETTLING TIME

The simplest method for PLL settling time measurement is monitoring the VCO tuning voltage waveform during the PLL locking process. In ideal case, this voltage is linearly proportional to the VCO frequency. Time interval needed for VCO tuning voltage to achieve a stable value after initiating the PLL frequency change, is equal to the PLL settling time. This method although very simple can rarely be used with integrated circuits. In integrated circuits with completely integrated on-chip PLL, VCO tuning voltage as

one of the most sensitive signals in the chip is seldom available outside the IC. Any noise or spurs coupled to the line carrying this signal can severely degrade the performance of the PLL and the complete system, which is the reason it's so rare available outside the transceiver IC.

The second approach of measuring the PLL lock time is to observe the signal at the output of the VCO feedback frequency divider inside the PLL. In this case, the time elapsed between triggering the VCO frequency change and the time at which desired feedback frequency is achieved (should be the same as reference frequency) is PLL settling time.

Frequency synthesizers inside the integrated circuits often have some kind of indicators that provide useful information about the state of PLL circuits. For example, usually there are digital and analog lock detectors, VCO tuning voltage comparators etc. Lock detectors indicate the user of IC if phase lock state has been achieved. VCO tuning voltage comparators are used to check if tuning voltage value is inside the specified range. Sometimes these indicators can be directly monitored by the user usually via GPIO pin of IC. These indicators are not too accurate but can be used to provide rough estimation of PLL settling time.

All of the previously described measurement methods require direct access to the internal signals of the PLL which are not needed in the normal operation mode. Also, routing of these signals to the output pins of IC carries a certain risk since unwanted coupling and performance degradation can happen.

## III. MEASURING THE PLL SETTLING TIME USING SPECTRUM ANALYZER

Main purpose of spectrum analyzer is to measure frequency spectrum of known and unknown signal. Many of spectrum analyzer devices today can make time domain and power statistics (CCDF) measurements beside frequency domain measurements, usually using alternative hardware path. Time-domain waveform measurements using spectrum analyzer with that option are comparable to a precision vector signal analyzer measurements. Both provide demodulated I/Q data for individual magnitude and phase analysis.

The basic idea is that user can derive phase and frequency error and calculate the exact value of PLL lock time from baseband I/Q data, sampled during PLL settling process. The block diagram of measurement setup that we used is shown in Fig.2.
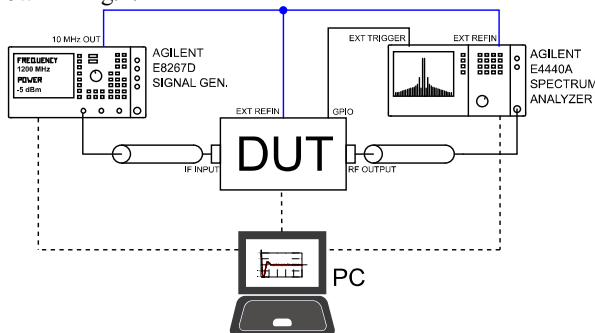


Fig. 2. Measurement Setup

Agilent E4440A 3Hz-26.5GHz spectrum analyzer [3] has been used for time-domain measurements. E4440A

spectrum analyzer down-converts output signal from the DUT and digitize the baseband signal providing I/Q samples that are post-processed on a PC. IF signal for the mixer inside the DUT is made using Agilent E8267D 250 kHz-20 GHz signal generator [4]. It is 1.2 GHz carrier with -5dBm power level. DUT up-converts IF signal and its output RF signal is connected to the spectrum analyzer input.

The DUT, used in the experiments, is evaluation board for CMOS RFIC transceiver with completely integrated frequency synthesizer that covers very wide frequency bandwidth. Simplified block diagram of DUT's RFIC is given in Fig.3.
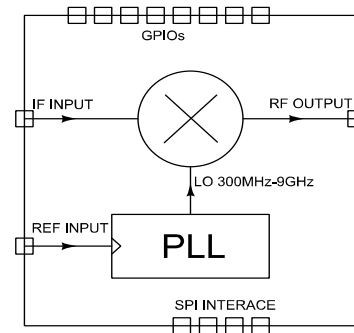


Fig. 3. RFIC-DUT Simplified Block Diagram

PLL inside the DUT is fractional-N mode synthesizer covering the range from 300 MHz to 9 GHz. The VCOs and loop-filter are fully integrated. PLL requires no external parts to cover the complete operating frequency range. Valid reference frequency values are between 10 and 70 MHz. In our measurements we used 40 MHz reference frequency coming from external ultra low-noise VCTCXO.

The chip is fully configurable via Serial Peripheral Interface (SPI). Some basic control options are also controllable via the chip GPIO pins.

Digital control logic implemented inside the DUT for configuration and control of PLL subsystem includes eight sets (profiles) of PLL control signal values. Active PLL profile can be selected with GPIO pins, SPI register value or a combination of these two. Additionally, each set of PLL control signals contains fast-lock settings for the PLL core, to facilitate faster frequency settling upon PLL profile change. This means that user can define the initial values for charge-pump current and loop-filter components during the programmable amount of time expressed in reference clock cycles for each PLL profile. The idea is to provide an option to increase the loop bandwidth of the PLL when locking process starts and reduce the total settling times of the synthesizer.

RFIC has several flexible GPIO pins which are individually programmable. GPIOs can be used in several ways, from basic input/output to advanced control of RF channels and PLL. When used as output, each GPIO pin can be configured to output values of PLL loop status indicators or Fast Lock Active signal. Fast Lock Active is a digital signal which takes high logic value, when user changes the active PLL profile and goes back low when fast-lock mode time expires, as explained in previous chapter.

This functionality has been used as a trigger for spectrum analyzer in our measurements. We used two PLL profiles to store PLL settings for two different PLL frequencies, $F_1$ and $F_2$. One GPIO pin is configured to output Fast Lock Active Signal. This signal is connected to the external trigger input

of spectrum analyzer. Before measurement PLL is locked to the first PLL frequency $F_1$. Central frequency of spectrum analyzer is set to the second PLL frequency value increased by the frequency value of IF signal coming from the signal generator $F_{IF} = 1.2$ GHz, since the DUT will perform frequency up-conversion. Alternative wideband IF path with 80 MHz bandwidth is selected in E4440A spectrum analyzer. This makes it possible to practically eliminate the error due to spectrum analyzer's IF filter transient behavior while measuring the PLL settling time. Sampling Rate is programmed to be 100 MHz. Digitizer inside the analyzer has 14-bit resolution. Agilent E4440A spectrum analyzer can store the maximum of 1 million samples in its internal memory. That means that time interval that can be observed is about 10 ms which should be quite enough since the PLL settling time of our DUT was expected to be bellow 100 µs.

Active PLL profile is then changed. PLL loop starts locking to the new PLL frequency and at the same moment Fast Lock Active signal triggers spectrum analyzer to start sampling the down-converted baseband signal. We locked the spectrum analyzer and the DUT to 10 MHz reference signal that comes out from the signal generator in order to completely eliminate the frequency error due to different reference sources used in different devices.

The complete measurement process is automated using Python modules and scripts. PC communicates via local network with used measurement equipment and over USB with the DUT. It configures spectrum analyzer [5], signal generator [6], programs the DUT and triggers the measurement process. When the spectrum analyzer is done with sampling, it sends raw I/Q samples of down-converted baseband signal to the PC.

Further signal processing is done on PC also using Python. Block diagram is presented in Fig.4 [7]. From I/Q samples, we first calculate the output phase as:

$$\Phi[n] = \arctan\left(\frac{Q[n]}{I[n]}\right) \qquad (1)$$

Unwrapped phase is then passed through the low-pass FIR filter. Pass-band frequency is chosen to be 700 kHz and stop-band frequency 1.4 MHz. This rejects wideband noise due to quantization and the rest of noise sources which are present in DUT and RF frontends of signal generator and spectrum analyzer. Pass-band width of 700 kHz is large enough not to affect the measurement accuracy since the PLL inside the DUT is configured to have the closed-loop bandwidth of around 360 kHz.
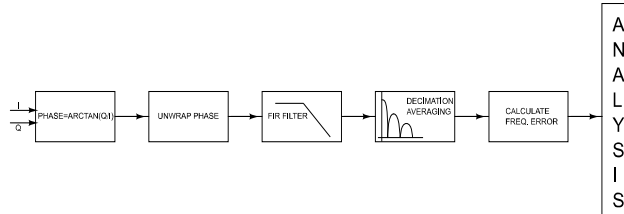


Fig. 4. RFIC-DUT Simplified Block Diagram

Last step in processing the phase signal is to perform the decimation using comb-filtering with averaging/smoothing factor of 40. Received signal instantaneous frequency can be calculated from its phase as:

$$F[n] = \frac{1}{2\pi} \frac{d\Phi'}{dt} = \frac{1}{2\pi} \frac{\Phi'[n] - \Phi'[n-1]}{\Delta T}, \qquad (2)$$

where $\Phi'[n]$ is the received signal phase after filtering and decimation at the output of the comb filter, and $\Delta T$ is the sampling interval. ADC sampling rate $SR$ is reduced by a decimation factor $K$, so the sampling interval at the output of comb filter is $\Delta T = K / SR$. Received signal instantaneous frequency is then:

$$F[n] = \frac{1}{2\pi} \frac{(\Phi'[n] - \Phi'[n-1]) \cdot SR}{K}. \qquad (3)$$

Since all of the devices in the measurement setup are synchronized, received signal frequency is equal to the PLL frequency error $F_{ERR} = F$. PLL settling time can be calculated as a time needed for frequency error to enter some predefined tolerance window, for example 10 ppm of targeted output frequency value as used in our measurements.

## IV. MEASUREMENT RESULTS

Results of PLL settling time measurements using the method described in the previous chapter will be presented here. First case that was measured is the PLL settling time after frequency change from 3.9 GHz to 4.0 GHz without fast-lock settings activated. The synthesizer's loop is configured to have approximately 360 kHz closed-loop bandwidth with 55 degrees phase margin. The PLL output frequency error is shown in Fig.5. PLL achieves lock after 12.5 µs.
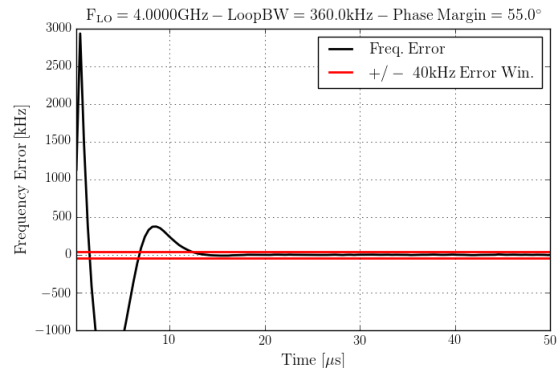


Fig. 5. PLL Frequency Settling from 3.9 to 4.0 GHz

Second case illustrates the PLL operation in fast-lock mode for 25 µs immediately after triggering frequency change from 3.9 to 4.0 GHz. During the fast-lock operation, PLL has around 650 kHz of loop bandwidth with 55 degrees phase margin. After fast-lock active time expires, the synthesizer's loop switch back to the settings which give around 360 kHz of loop bandwidth with the same phase-margin. The PLL locking process in this case is illustrated in Fig.6. During the fast-lock mode operation, PLL settling is clearly accelerated compared to previous case, due to wider loop bandwidth, and PLL achieves lock around 7.5 µs. In 25th µs after triggering the frequency change, PLL sets back from the fast-lock mode settings to the normal operation mode. At that time point PLL's charge-pump current and some loop-filter components abruptly change their values. This introduces frequency glitch which is also captured and clearly shown in Fig.6. The proposed measurement method can also be used in the process of optimizing the PLL settings to minimize the amplitude of that glitch in output frequency.
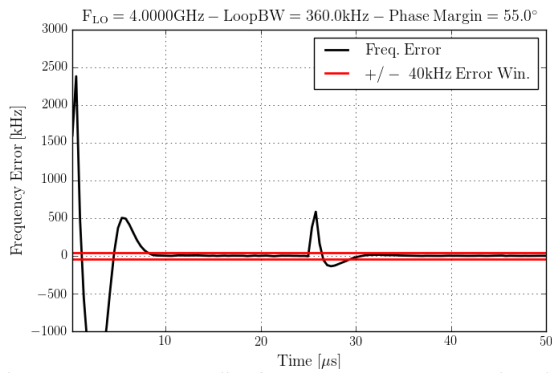
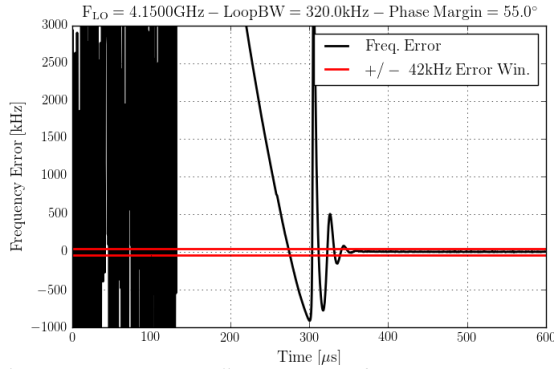Fig. 6. PLL Frequency Settling from 3.9 to 4.0 GHz, Fast-Lock mode during initial 25 µs
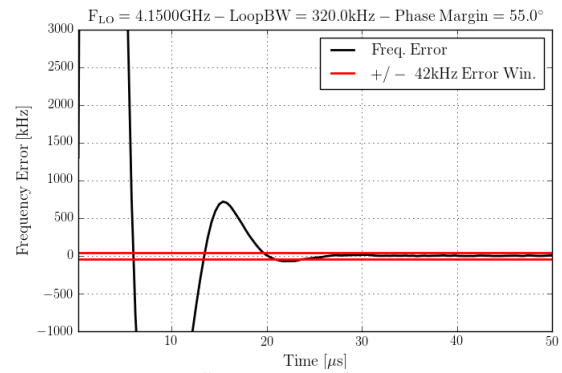


Fig. 8. PLL Frequency Settling to 4.15 GHz from Power-Down State, With Bias Noise Filter Bypassed

With VCO bias noise filter enabled, PLL settles to the targeted frequency from power down state finally after 370 µs. This is clearly a problem since it's more than 10 times increase in normal settling times shown in first two measured cases. Usual solution for this problem is to bypass the noise filter during the time VCO needs to start oscillating after power-up. This solution is implemented in the DUT we used. PLL settling time to 4.15 GHz output frequency after power-up, with VCO bias noise filter bypassed is presented in Fig.8. With these settings, PLL achieves lock for approximately 24 µs after power up.

## V. CONCLUSION

This paper demonstrates one possible method for measuring the settling time of a PLL-based frequency synthesizer. Signal analysis capabilities of Agilent E4440A 3 Hz-26.5 GHz spectrum analyzer were used to digitize the demodulated output signal of DUT. PLL's output frequency error was extracted from I/Q samples by simple post-processing of results using Python programming language on a PC. The results showed that various effects during PLL settling can be captured and quantified with proposed measurement method.



Fig. 7. PLL Frequency Settling to 4.15 GHz from Power-Down State, With Bias Noise Filter Enabled

Using the described measurement method, some other interesting effects can also be observed. For example, PLL user can often be interested in PLL settling time to some frequency from the power-down state. PLL inside the RFIC DUT we used in our experiments has integrated VCO cores which have one common bias circuit with noise filter. The noise filter is usually passive RC low-pass filter which serves to filter out the noise that comes from bias network. This noise often can completely ruin the phase-noise performance of a VCO circuit. On the other hand, the noise filter with very low pass-band frequency, as is the case in our DUT, increases a lot the time needed for PLL settling after power-up. This is clearly shown in Fig.7, where PLL locking to the 4.15 GHz output frequency after PLL power-up with enabled bias noise filter is presented. PLL is configured in this case to have around 320 kHz loop bandwidth with 55 degrees phase margin.

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