Ultra-Low Power, Sub-threshold Design - From Watch Microelectronics to IoT Integrated Circuits

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Abstract-In the era of battery operated devices, in particular booming wearables and Internet-of-Things (IoT) objects, ultralow energy consumption is becoming the most important challenge in the electronic design. Supply-voltage scaling is an efficient way to reduce energy by lowering the operating voltage. The reported Minimum Energy Point (MEP), in i.e. modern CMOS 65nm, can be as low as 0.35V. To achieve such low voltage operation, sub-threshold circuit design needs to be considered. Swiss watch microelectronics was exploring this approach since 1970. An overview of the principles and challenges of today's sub-threshold design will be given in this paper. The paper depicts also the 50 years of the Swiss "Quest for the Holy Grail" in ultra low-power wearable electronics, started with the world's first electronic quartz wrist watch BETA1 (1967) developed by the Centre Electronique Horloger (CEH) in Neuchâtel, toward autonomous, batteryless IoT objects of tomorrow.

Index Terms—Sub-threshold design; Watch microelectronics; Integrated circuits; IoT

I. THE FIRST ELECTRONIC QUARTZ WATCH



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Key elements [1]



Module of the first

commercial watch

developed at

CEH



First LSI circuit developed for a wristwatch (110 components, 8.7mm², 12µA at 1.3V)

Miniaturized quartz First prototype of 8192Hz small size resonator developed at CEH.

Module illustration



on the right: the **printed circuit** with the **IC** and the **quartz**

electromechanical part

on the left:

First electronic quartz watch - Realizations

• The miniaturized quartz resonator

- The geometry of the resonator must assure an ideal mechanical vibration of the quartz. Designed to
 avoid loss of energy and assure a resistance to shocks.
- The electronic circuit
 - 3 functions : maintenance of the vibrations of the quartz, division of the frequency and command of the display.
- The microelectronic technology
- New technology of integrated circuits born in the USA in 1958, adapted.
- Later, new microelectronic technology (CMOS) exploited allowing a drastic reduction of electrical consumption.

Wristwatch - A first electronic wearable device?

wearable technology

Examples



Characteristics:

- Battery operated, miniaturized electronic device, worn or carried on the body
 - Integrated low-power electronics

Secret project



The CEH prototype [2]

CEH (since 1962) -> CSEM (since 1984) Centre Electronique Horloger (CEH) Centre Suisse d'Electronique et de Microtechnique (CSEM)

II. FROM BATTERY-LIGHT TO BATTERY-LESS

And today?

50 years later ...

Power and miniaturization challenge remains!

... from battery-light to battery-less

Power challenge for Internet of Things (IoT)



CSEM Vision : From wireless to batteryless



Ultra-low energy consumption

- becoming the most important challenge in the electronic design
- supply-voltage scaling (an efficient way to reduce energy)
 - extreme low supply operation below MOS threshold voltage

-> "sub-threshold"/"week inversion" circuit design techniques!

- Swiss watch microelectronics was exploring this approach since the end of '60s
- hundred of millions of week inversion ICs been produced for watch applications

III. SUB-THRESHOLD DESIGN

Pioneering weak inversion for analog CMOS [1]





 First measurement of a MOS transistor at very low current (1967, by Eric Vittoz)

 Sub-threshold voltage experiments

EKV Model (Low Power MOSFET Model) [3]

- Advanced MOSFET model for lowvoltage low-current circuit design
- As supply voltage of circuits decreases to reduce power consumption
 - analog designs require a more physical, accurate and continuous compact MOS model.

=> Enz-Krummenacher-Vittoz (EKV) model

(http://ekv.epfl.ch/)

Modeling [3]



 $\begin{array}{c} & {}^{I}{}_{D}{}^{C0} & V_{P} = \text{pinch-off voltage} \\ \text{equipotential channel} (V_{D}{}^{=}V_{S}, I_{D}{}^{=}0) & V_{J} = \text{"forward junction voltage} \end{array}$

CMOS technology scaling



CMOS supply voltage scaling: Challenge to operate at 0.4V!

Categories Tear



Poarer	Energy source		٠	8+8	8+H	8+11	8+H	8+H	8+8
	(B - battery; H - emergy harvesting)	- T.							
	Lowest VDD Used By Components (V)	0.8	0.75	0.7	0.05	0.65	0.55	0.45	0.4
	Deep suspend current of MCU (inA)	100	72	52	38	27	20	14	30
	Conversion efficiency of DC-to-DC Conversion [%]	80%	82%	86N	88%	89%	91%	93%	951
	Spatial Power Density of DC Converter (W/www ¹)	1	1.17	1.36	1.59	1.85	2.16	2.52	2.9
	Peak Current Consumed by Connectivity Interface (mA)	50	19.2 8	7.44	2,87	1.11	0.43	0.16	0.0
	Transmission Power per bit (pW/bit)	2,48	0.97	0.38	0.14	0.0%	0.02	0.00	4
Form factor	Module footprint (mm2)	500	500	280	179	115	73	47	30
Performance	MCU Number of Cores	1	1	1	1	1	1	1	1
	MCU Current / Operation frequency (mJly/MHz)	90	21.7	15.7	11.3	8.9	7.7	6.7	5.8
	Max MCU (requency (MHz)	200	235	277	336	316	327	338	35
	MCU Flash size (KB)	\$124	1024	2048	4095	4096	8192	8192	819
	MCU Obrystone MIPS (DMIPS)	200	242	293	354	429	519	628	79
Peripheral	teamber of sensors integrated to system.	4		10	12	12	13	13	13
	Max Service Power (uW)	2850	1897	1009	729	617	522	442	37

Sensors will populate the world of IoT

Source: 2015 ITRS "IoE" roadmap [4]

2015 2017 2019 2021 2021 2025 2027 2029

Design considerations in week inversion [5-7]

- Exponential I-V characteristics in week inversion
 - PVT variations Not only an issue for analog!
 - Small variation on process (i.e. Vt)
 - exponential variation on the bias current
 - Temperature effects

Matching

- Current matching degraded
- Voltage matching improved

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Circuit building blocks to support sub-threshold digital design [8-9]

These basic blocks: Standard cell library ~ RAM ~ V_{DD} 1 Level shifters 1 Pads 1 Power Managemen Libraries can be optimized for several criteria: W/L • The lowest possible supply voltage The lowest possible leakage while supporting a target frequency



Embedded Computation & Control: 0.4V µ-controller [10]



Module and remote power

Nano Retina implant location in the retina



Nano Retina implant location in the eye

Week inversion retina ASIC - block diagram & pixel layout [12]





Using CMOS in weak Inversion

- To reach 100nA range of total IC power consumption:
 - All the functions of the retina built with MOS in weak inversion
 - All voltages scaled to in terms of $nU_{\tau} \sim 32 \text{ mV}$
 - One decade of current corresponds to a gate voltage increase of nU₇ln(10) = 2.3 nU₇

• Weak inversion:
$$\begin{split} I_{Drat} = I_s \exp & \left(\frac{V_G - V_{T0}}{n U_T} \right) \\ U_T = \frac{kT}{2} = 26.7 \, \mathrm{mV} \, \mathrm{at} \, T = 37^\circ \mathrm{C} \end{split}$$



IV. ULP IOT CONNECTIVITY

What about IoT?

- ... is growing fastly (remeber the ITRS Sensor roadmap)
- ... the sub-threshold activity (targeting IoT) becomes increasingly attractive Ambiqmicro, MIE Fujitsu Semiconductor with CSEM etc.

a 5mW Bluetooth Low Energy Transceiver

The first true 1V BT 5 LE silicon IP, functional down to 0.9V





- Following the ULP design watch microelectronics philosophy
- Toward today's connected objects and future IoT nodes

V. CONCLUSION

- 50 years of the Swiss "Quest for the Holy Grail" in ULP wearable electronics, based on the <u>low-voltage</u>, weak inversion and sub-threshold
- From the world's first electronic quartz wristwatch BETA 1 until today, several generations of researchers have built & evolved micro-power design techniques:
 - from 10μm to 28nm semiconductor process
 - from bipolar logic to RF CMOS
 - from 100 transistor LSI to multi million transistor SoCs
- Heading toward autonomous, batteryless IoT objects of tomorrow.

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